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semiconductor <sup>TM</sup>

CUSIIC

MPC8536 DEVELOPMENT PLATFORM  
CALAMARI

FREESCALE

DATE: Fri Aug 01 13:44:45 2008

PROJECT: CALAMARI

ENGINEER: MICHAEL GEORGE

REV B.1

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SCHEMATIC HISTORY

R.0	INITIAL VERSION FOR RE-SPIN
R.0	CORRECTS ALL KNOWN ERRATA (CE1-CE5)
R.0	ADDED VBUS PROTECTION RESISTORS
R.0	CONNECTED CONFIG_5[16:15] TO FXGA
R.0	ADDED TWO TESTPOINTS TO THE FXGA
R.0	DATABLIZZARD INTD MOVED FROM INTA TO INTD
R.0	ADDED ESATA SSD PROTECTION
R.0	VBUS POWER FOR USB3 REMOVED FROM 2077
R.0	PCI_CLK CPG RAN THROUGH POR BUFFERS
R.0	REMOVED 1.5V LED
R.0	ADDED FILTER CAP & RESISTORS TO AD17561
R.0	SEPARATED VCCORE ENABLES
R.1	ADDED GROUND TO U134-PIN #9

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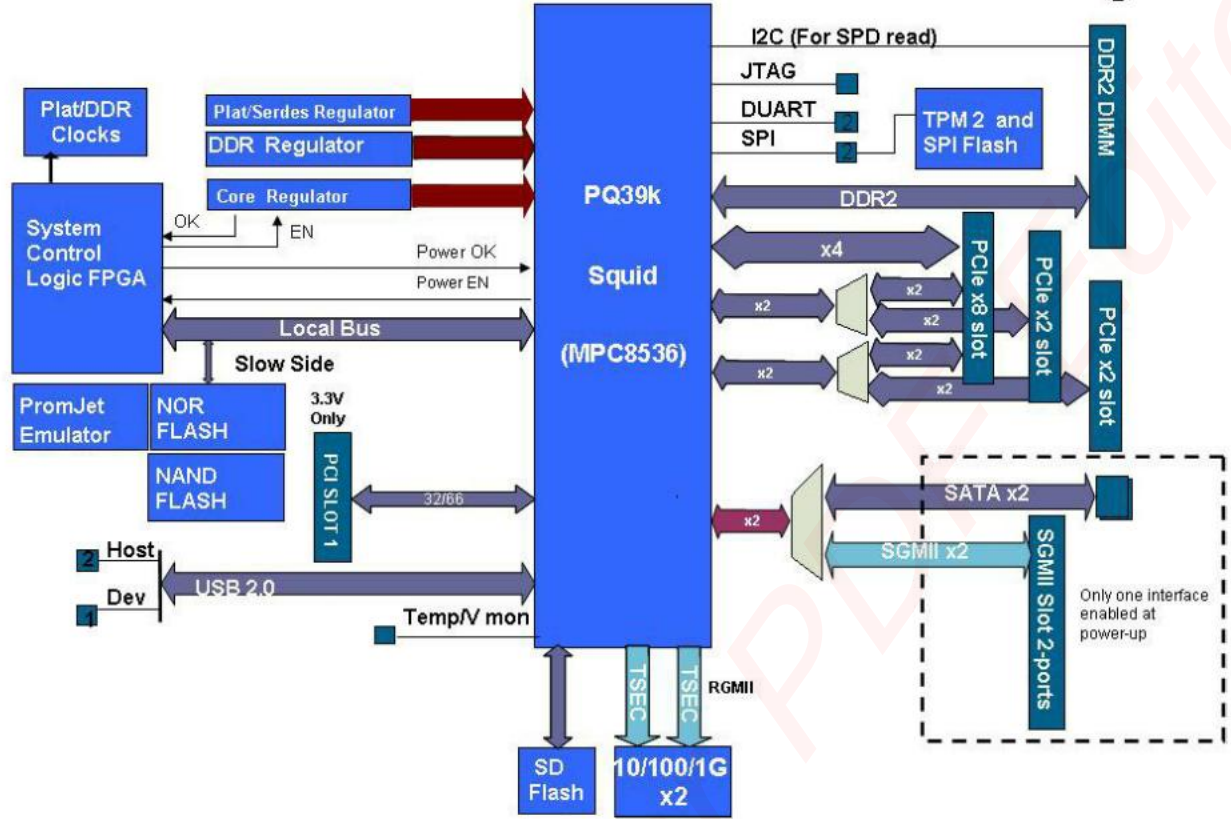
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# FSL Calamari Block Diagram



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# PCB STACKUP

Lay #	Thick (in)	Picture	Type Dk Df	Description	Drill Picture
0.0007/0.0007			3.20	Soldermask	
1	0.0022		F	1/2oz w/plating	
	0.0040		4.40 0.018	fill	
2	0.0013		P	1oz	
	0.0080		4.47 0.018	core	
3	0.0013		P	1oz	
	0.0053		4.47 0.018	fill	
4	0.0006		S	1/2oz	
	0.0120		4.49 0.018	core	
5	0.0006		S	1/2oz	
	0.0053		4.47 0.018	fill	
6	0.0013		P	1oz	
	0.0080		4.47 0.018	core	
7	0.0013		P	1oz	
	0.0053		4.47 0.018	fill	
8	0.0006		S	1/2oz	
	0.0120		4.49 0.018	core	
9	0.0006		S	1/2oz	
	0.0053		4.47 0.018	fill	
10	0.0013		P	1oz	
	0.0080		4.47 0.018	core	
11	0.0013		P	1oz	
	0.0040		4.40 0.018	fill	
12	0.0022		F	1/2oz w/plating	
0.0007/0.0007			3.20	Soldermask	

0.0927 Total thickness (in) Over metal (with solder mask)  
 0.0881 After lamination thickness (in)  
 0.0883 Over laminate thickness (in) (with soldermask)  
 0.0930 Customer Requirement (in)  
 +/-0.0090 Customer Tolerance (in)

## Impedance Constraint Information

Imp #	Imp Name	Picture	Affect Layer (1) (2)	Line Width (1) (2)	Center-to-Center (1) (2)	Ref Plane Top Bot	Targ ohms	Tol ohms	tpd ns/in	Atten dB/in	Predict ohms
1	Surf MS		1 None	0.005		None 2	55	5	153	0.24	54.41
2	Surf MS		1 None	0.006		None 2	50	5	154	0.23	50.00
3	EC MS		1 None	0.0045 0.0045	0.0115	None 2	100	10	153	0.24	99.76
4	Stripline		4 None	0.006		3 6	50	5.5	179	0.28	51.41
5	Stripline		4 None	0.005		3 6	55	5.5	179	0.28	55.65
6	EC SL		4 None	0.004 0.004	0.008	3 6	100	10	184	0.30	93.90
7	EC SL		4 None	0.005 0.005	0.0125	3 6	100	10	181	0.29	96.35
8	Stripline		5 None	0.005		3 6	55	5.5	179	0.28	55.65
9	Stripline		5 None	0.006		3 6	50	5	179	0.28	51.41
10	EC SL		5 None	0.004 0.004	0.008	3 6	100	10	184	0.30	93.90
11	EC SL		5 None	0.005 0.005	0.0125	3 6	100	10	181	0.29	96.35
12	Stripline		8 None	0.006		7 10	50	5	179	0.28	51.41
13	Stripline		8 None	0.005		7 10	55	5.5	179	0.28	55.65
14	EC SL		8 None	0.004 0.004	0.008	7 10	100	10	184	0.30	93.90
15	EC SL		8 None	0.005 0.005	0.0125	7 10	100	10	181	0.29	96.35
16	Stripline		9 None	0.006		7 10	50	5	179	0.28	51.41
17	Stripline		9 None	0.005		7 10	55	5.5	179	0.28	55.65
18	EC SL		9 None	0.004 0.004	0.008	7 10	100	10	184	0.30	93.90
19	EC SL		9 None	0.005 0.005	0.0125	7 10	100	10	181	0.29	96.35
20	Surf MS		12 None	0.005		None 11	55	5	153	0.24	54.41
21	Surf MS		12 None	0.006		None 11	50	5	154	0.23	50.00
22	EC MS		12 None	0.0045 0.0045	0.0115	None 11	100	10	153	0.24	99.76

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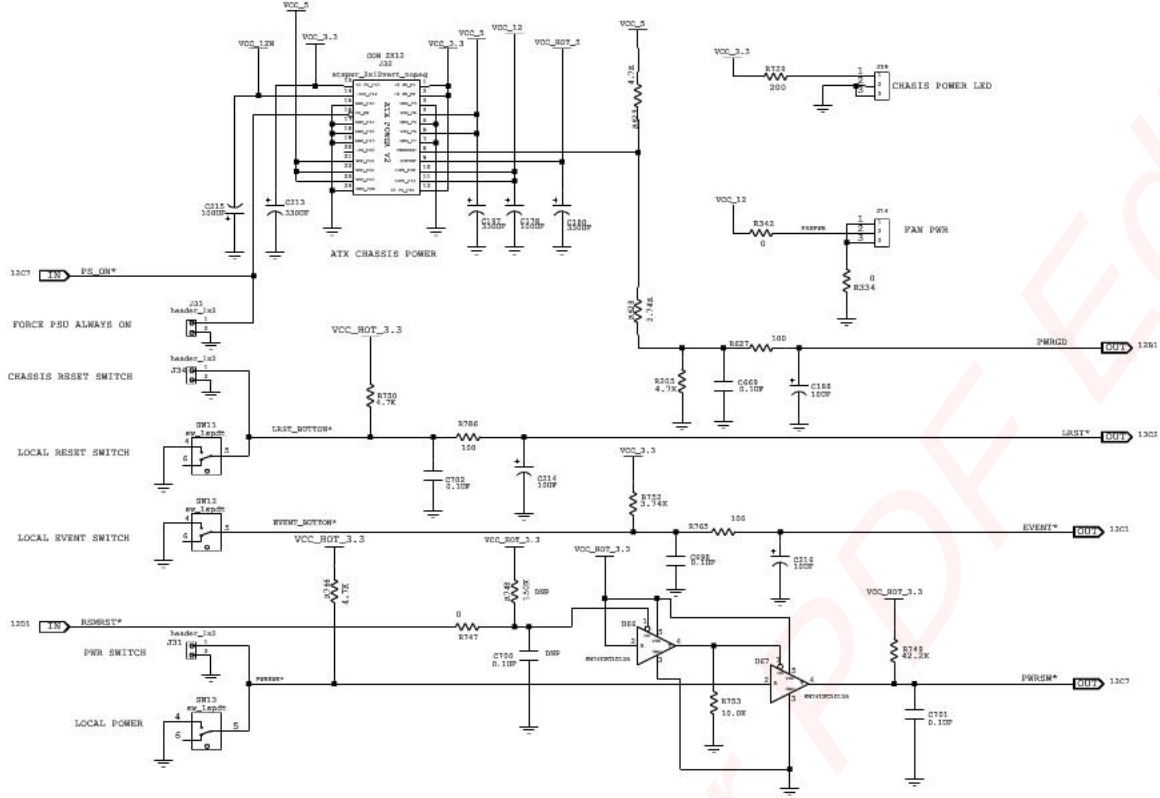
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# POWER ENTRY, USER SWITCHES



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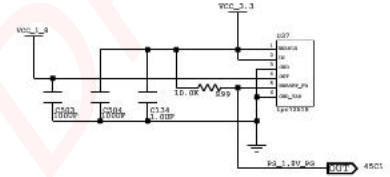
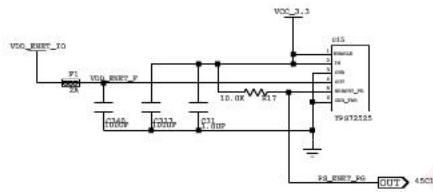
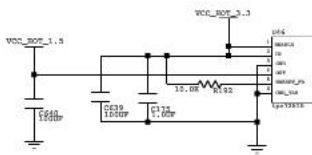
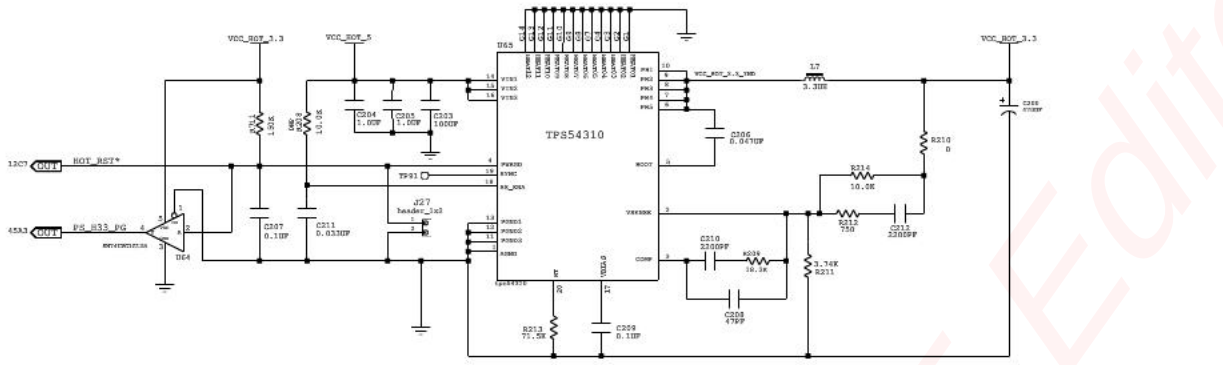
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# HOT POWER SUPPLIES



Worst Case  $I/O < 1.5A$  ( $P = 1.6A * 2.5V$ ).  
Copper Area = 1 cm sq

POWERS ONLY THE SITE SIGNAL NETWORKS (...LESS THAN 20MHz)  
As such, ONLY THE BASE MINIMUM PCB COPPER AREA IS NEEDED.

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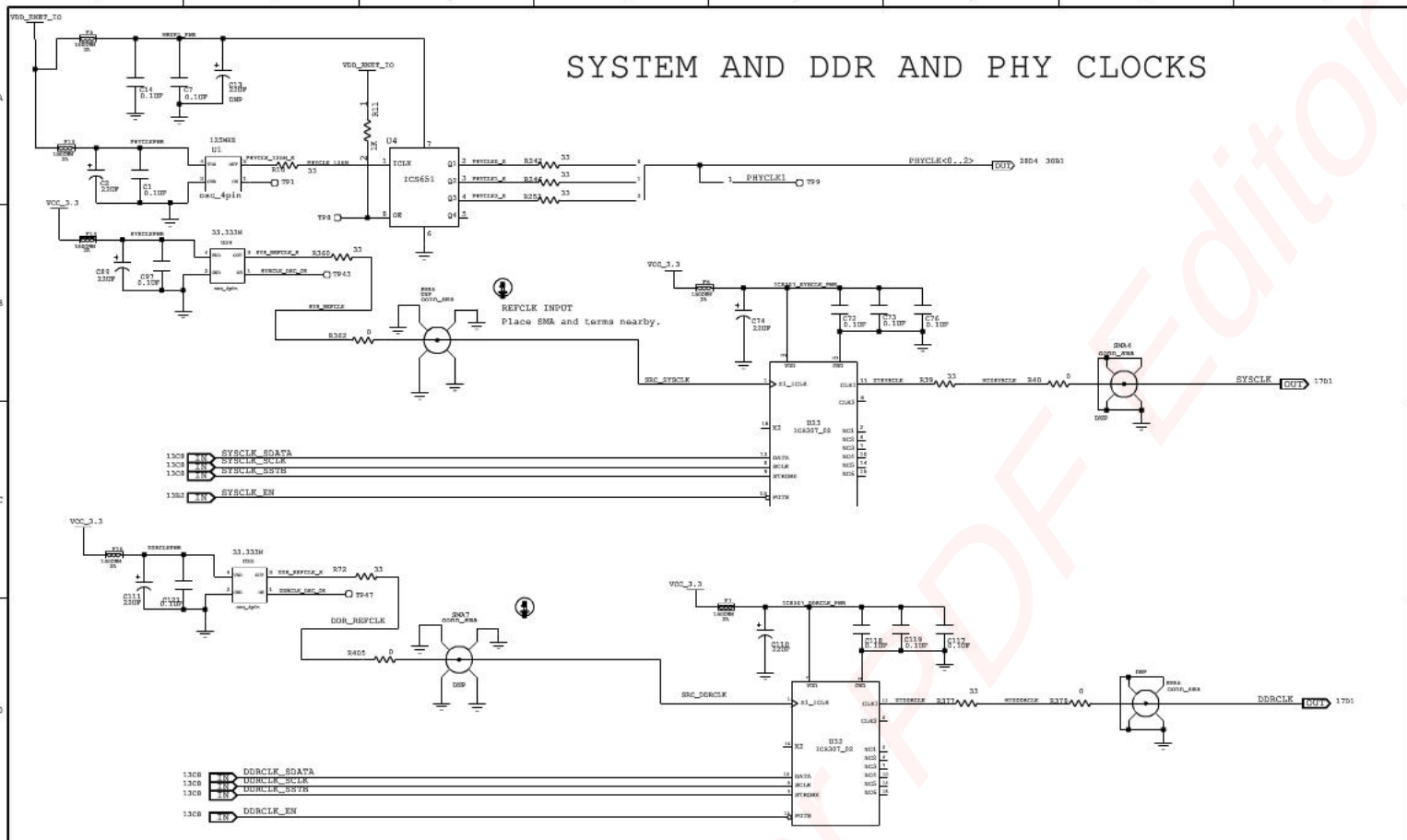
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# SYSTEM AND DDR AND PHY CLOCKS



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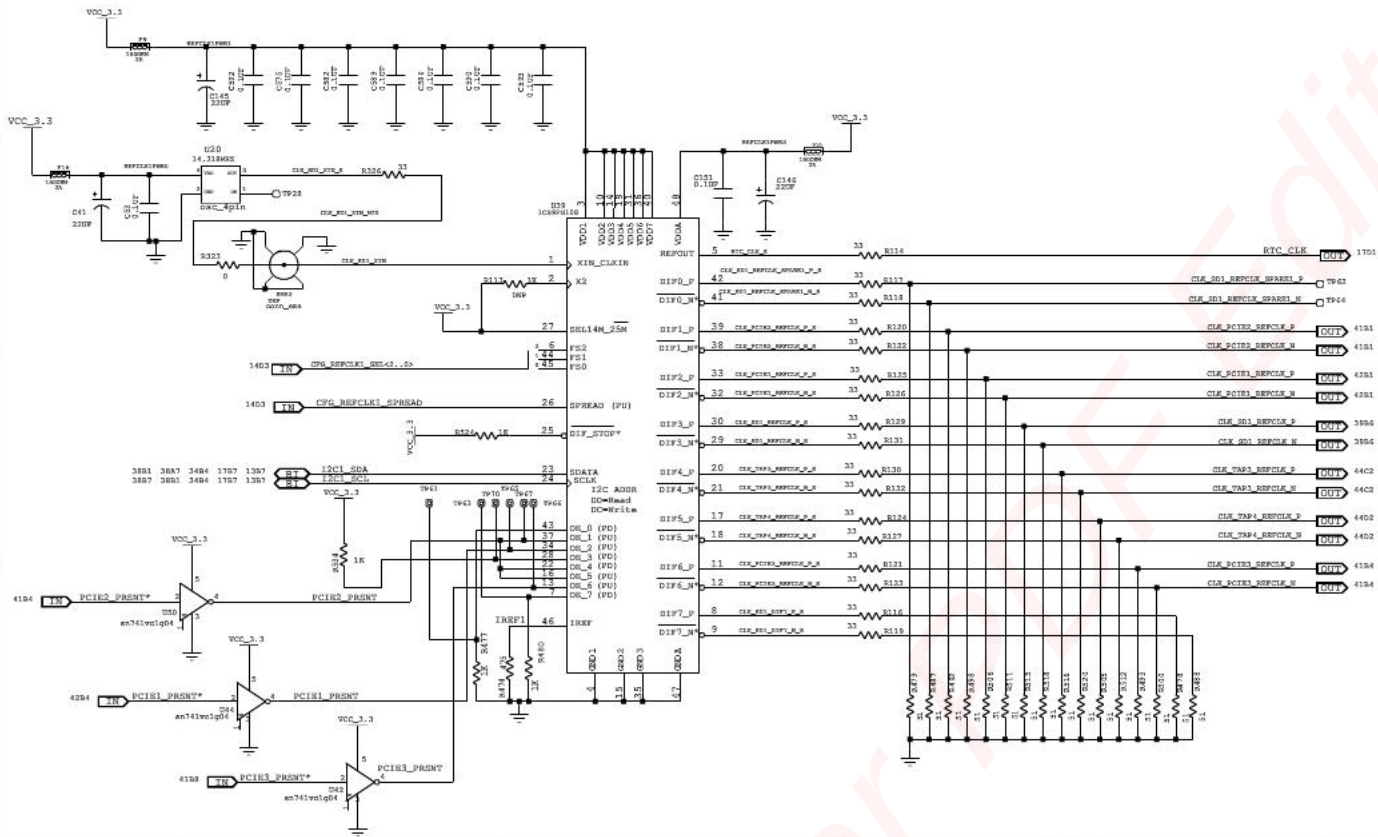
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# SERDES 1 CLOCK



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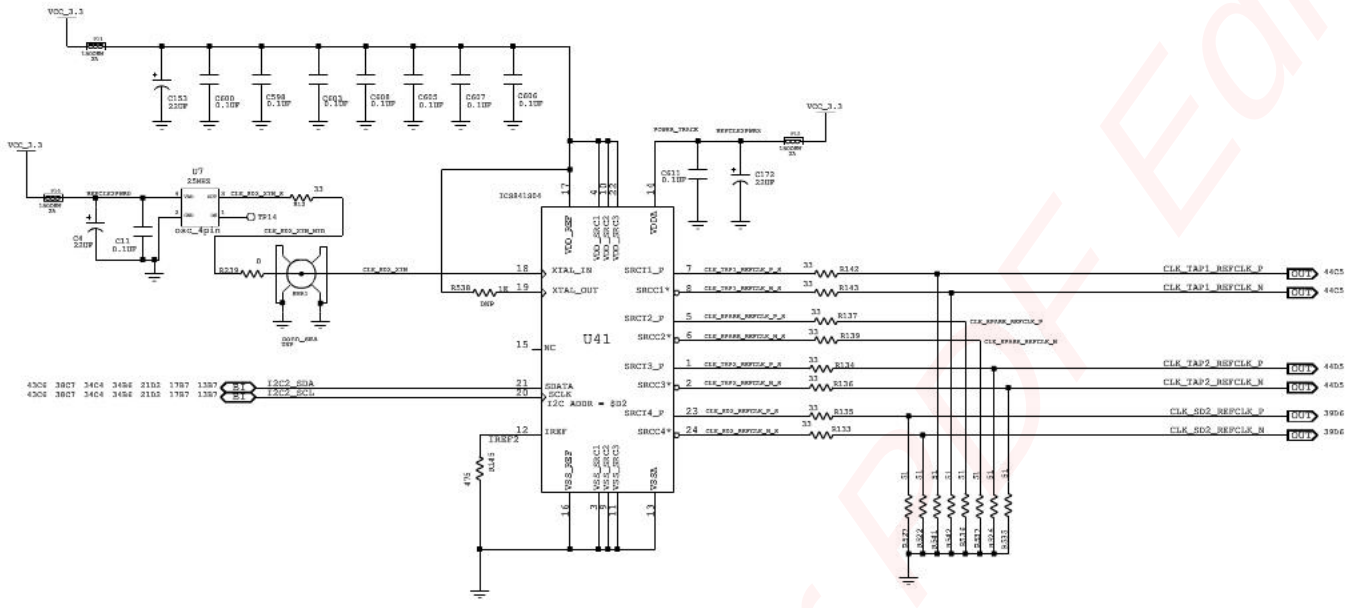
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# SERDES2 CLOCK



FREESCALE

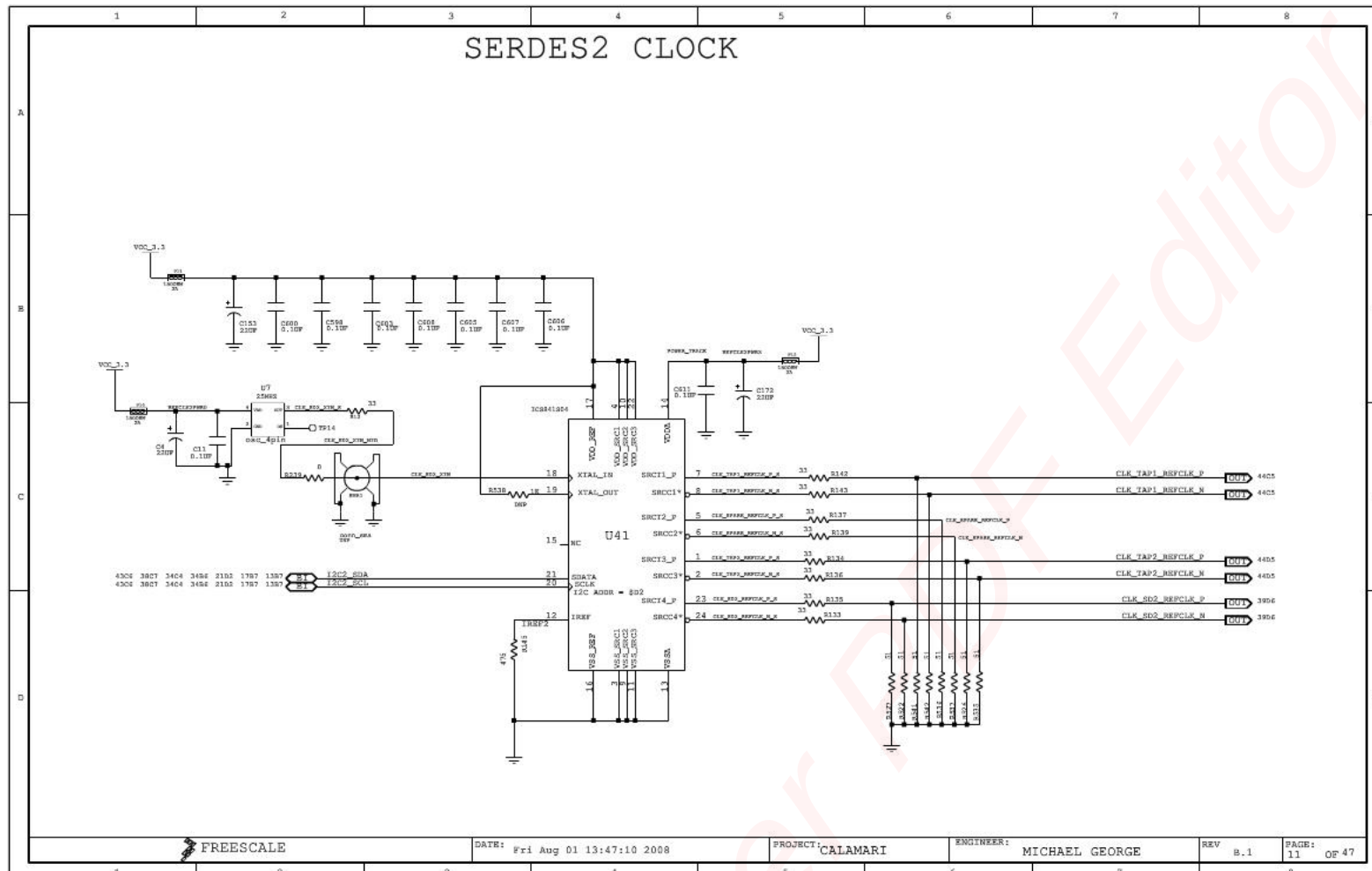
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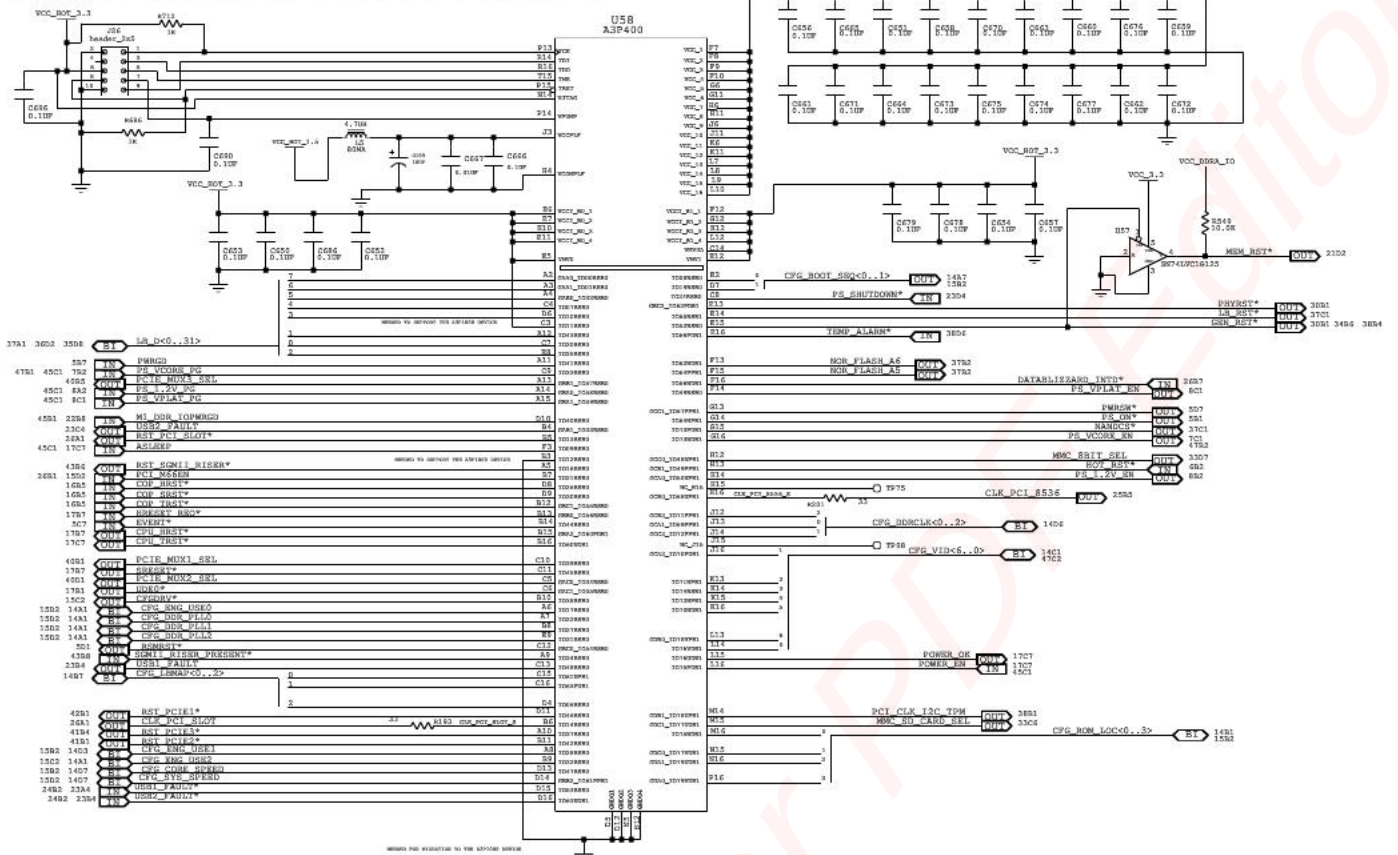
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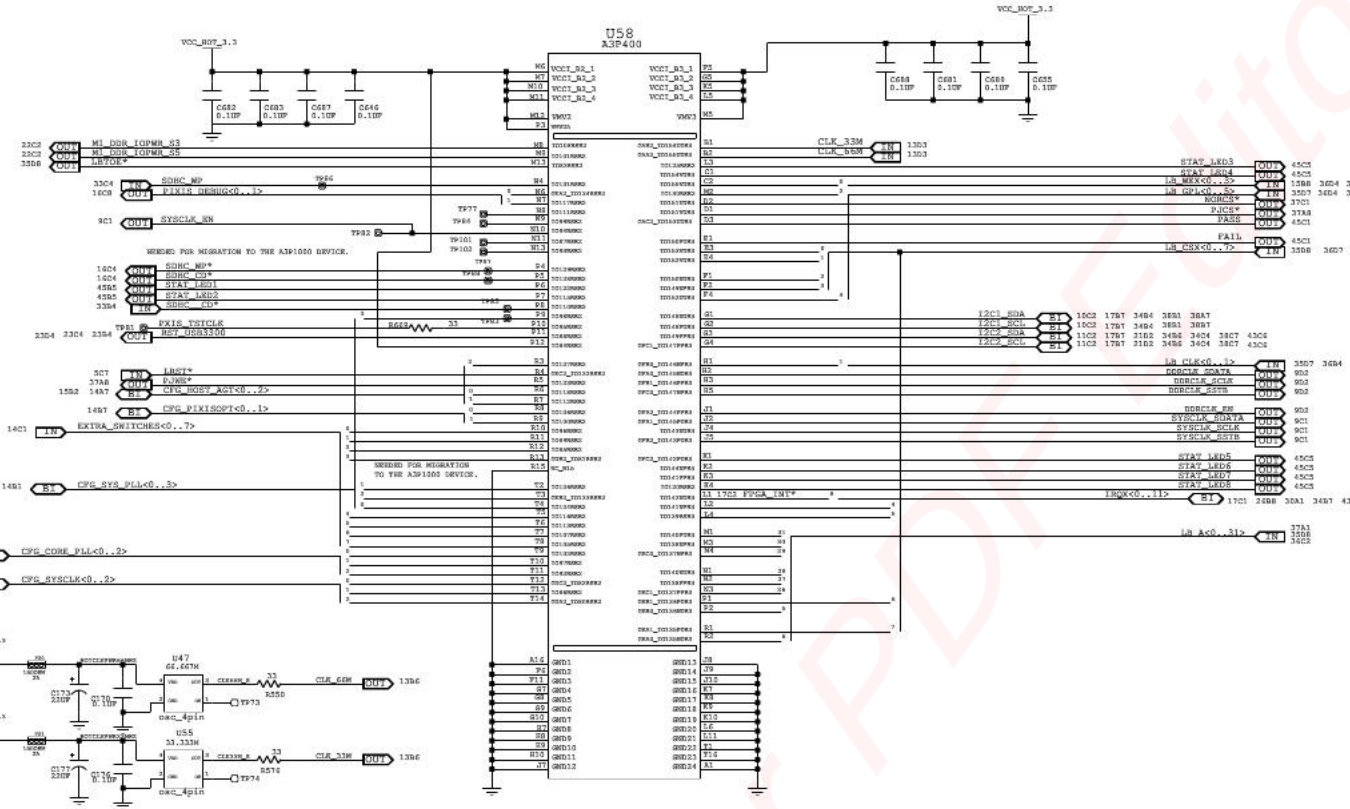
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# PIXIS SYSTEM LOGIC PART 1



# PIXIS SYSTEM LOGIC PART 2



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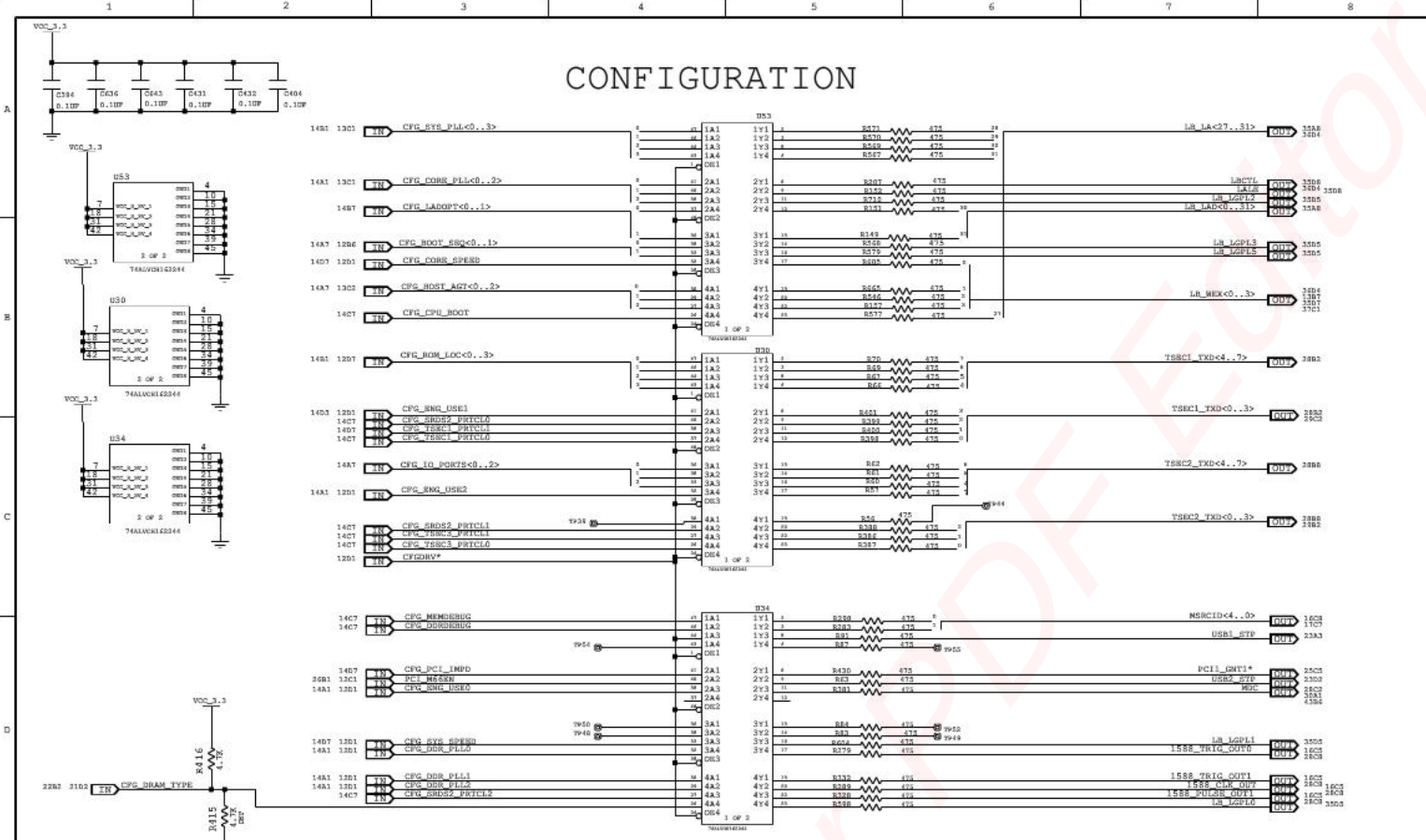
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# CONFIGURATION



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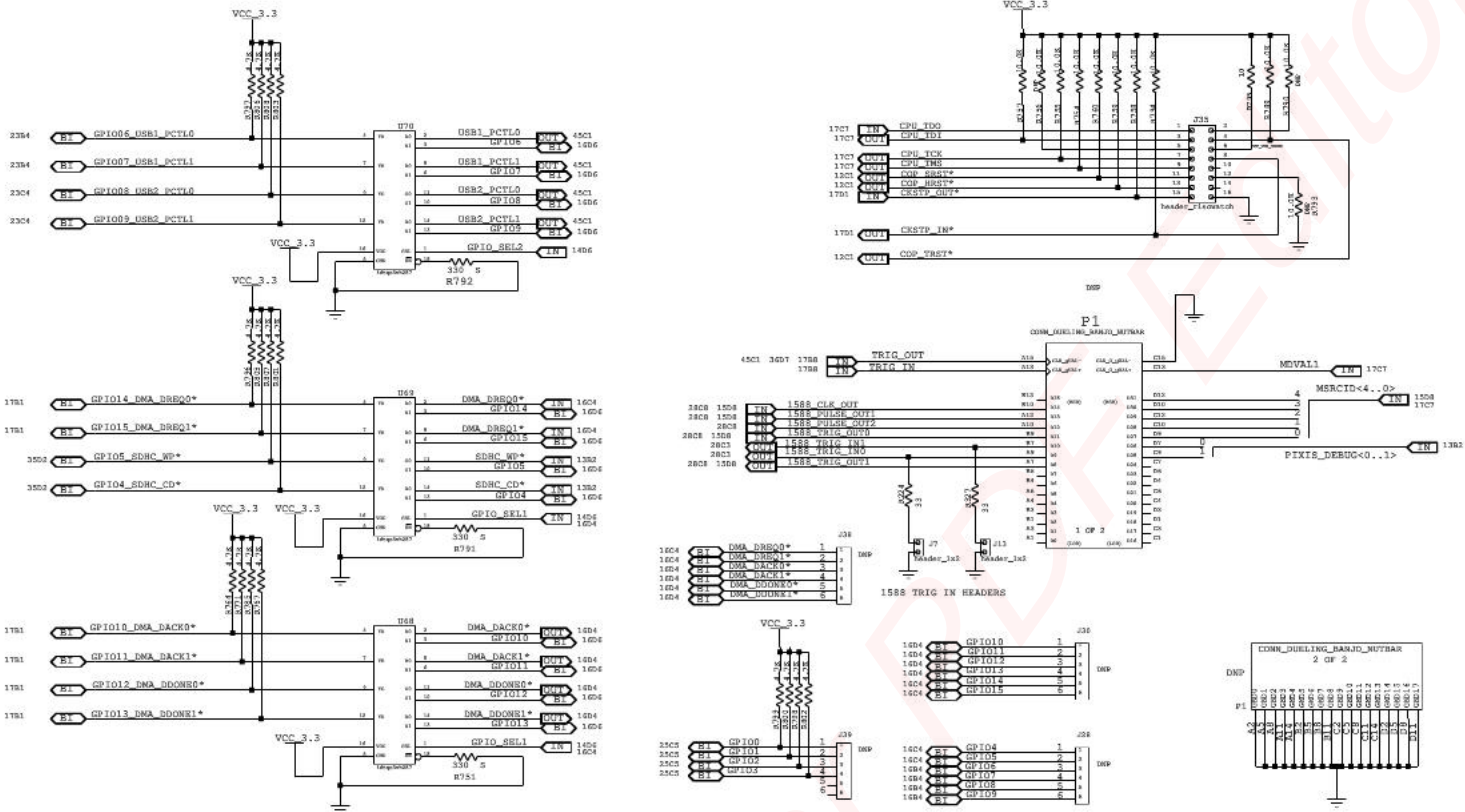
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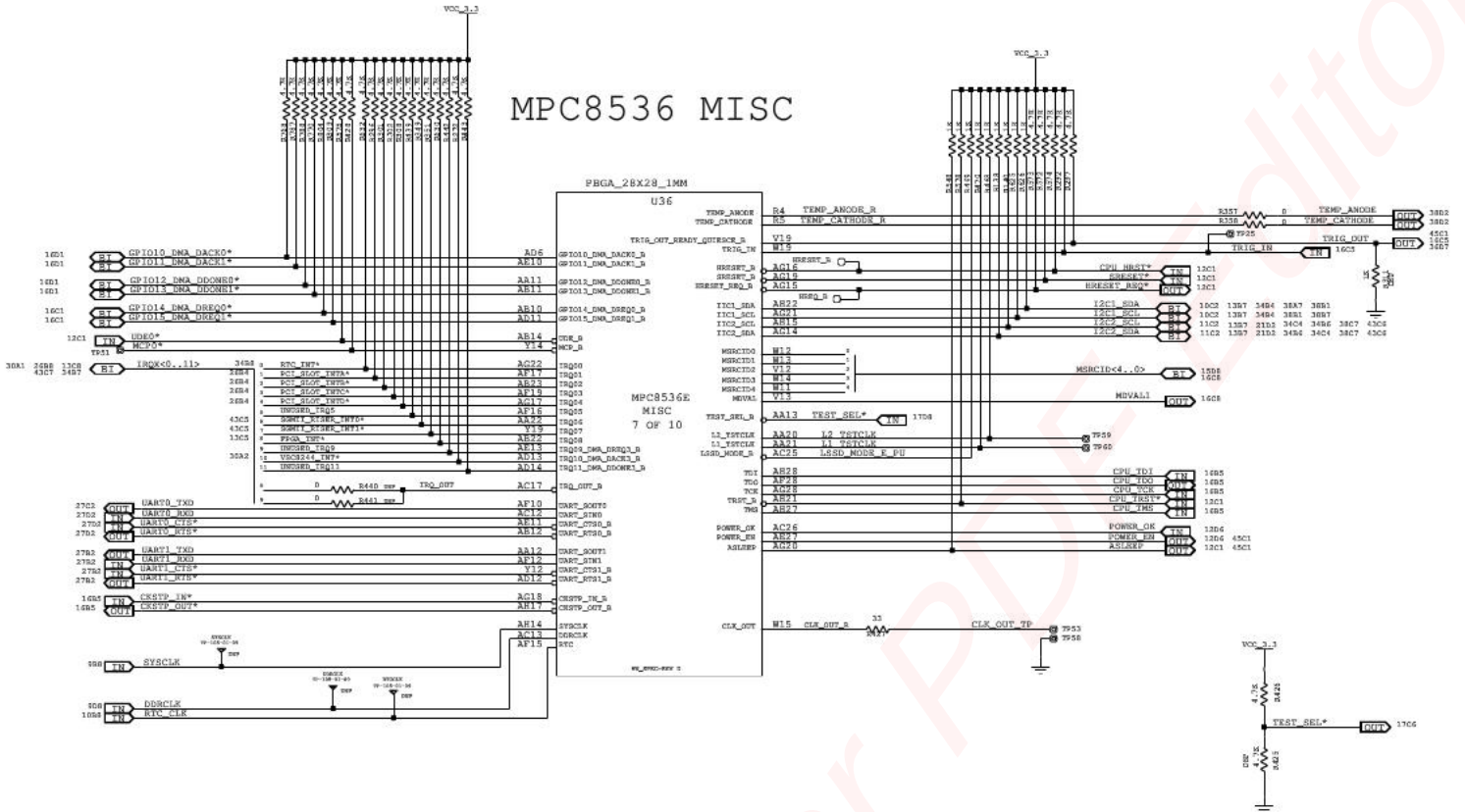
# JTAG/COP, GPIO, AND 1588 HEADERS



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# MPC8536 MISC



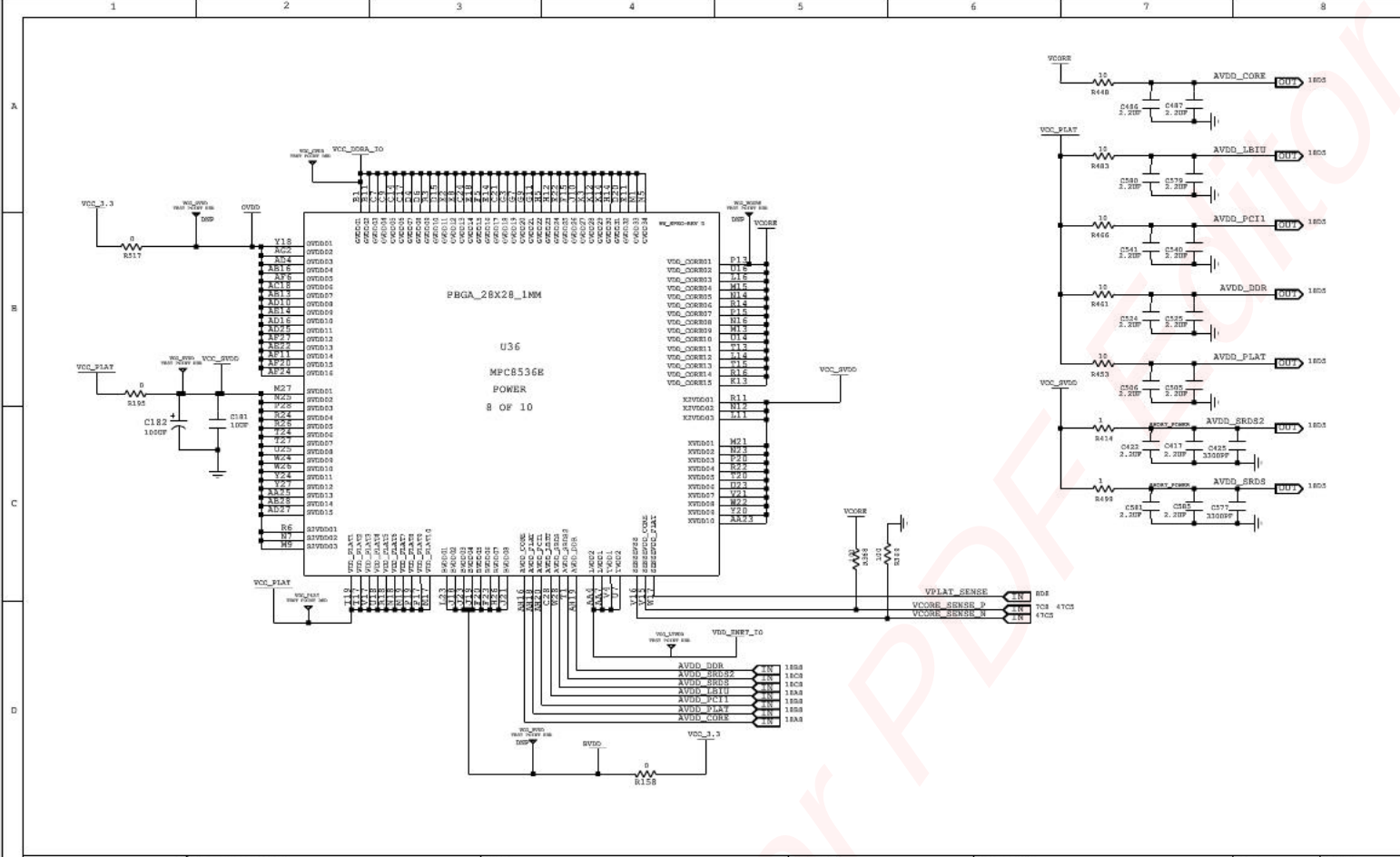
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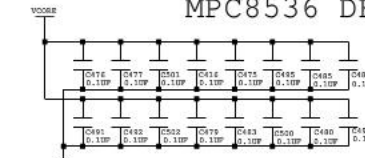
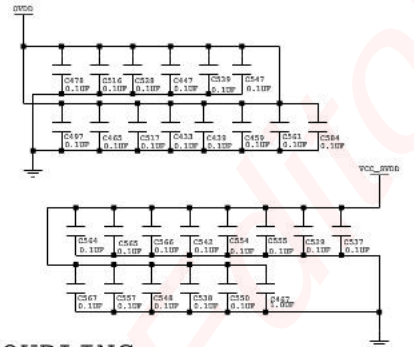
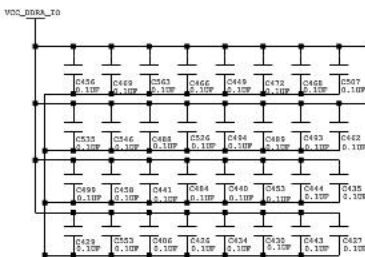
PCGA\_26X28\_1MM

# MPC8536 GND

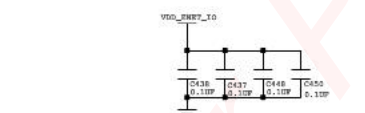
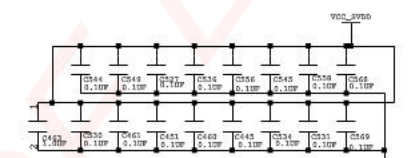
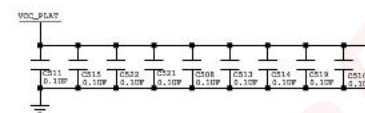
Pin	Signal	Package Pin	Signal	Package Pin
D5	DM01	DM01	M28	DM01
P4	DM02	DM02	M25	DM02
D26	DM03	DM03	M24	DM03
D23	DM04	DM04	M27	DM04
C12	DM05	DM05	M26	DM05
C13	DM06	DM06	M28	DM06
D20	DM07	DM07	M22	DM07
D19	DM08	DM08	M25	DM08
B10	DM09	DM09	M24	DM09
A2	DM10	DM10	M26	DM10
B3	DM11	DM11	M28	DM11
F21	DM12	DM12	M24	DM12
F22	DM13	DM13	M25	DM13
F23	DM14	DM14	M27	DM14
F24	DM15	DM15	M26	DM15
A3	DM16	DM16	M28	DM16
F18	DM17	DM17	M22	DM17
D15	DM18	DM18	M25	DM18
D17	DM19	DM19	M24	DM19
A4	DM20	DM20	M26	DM20
F21	DM21	DM21	M27	DM21
B1	DM22	DM22	M28	DM22
C12	DM23	DM23	M24	DM23
C13	DM24	DM24	M25	DM24
D20	DM25	DM25	M22	DM25
D19	DM26	DM26	M25	DM26
B10	DM27	DM27	M24	DM27
A2	DM28	DM28	M26	DM28
B3	DM29	DM29	M28	DM29
F21	DM30	DM30	M24	DM30
F22	DM31	DM31	M25	DM31
F23	DM32	DM32	M27	DM32
F24	DM33	DM33	M26	DM33
A3	DM34	DM34	M28	DM34
F18	DM35	DM35	M22	DM35
D15	DM36	DM36	M25	DM36
D17	DM37	DM37	M24	DM37
A4	DM38	DM38	M26	DM38
F21	DM39	DM39	M27	DM39
B1	DM40	DM40	M28	DM40
C12	DM41	DM41	M24	DM41
C13	DM42	DM42	M25	DM42
D20	DM43	DM43	M22	DM43
D19	DM44	DM44	M25	DM44
B10	DM45	DM45	M24	DM45
A2	DM46	DM46	M26	DM46
B3	DM47	DM47	M28	DM47
F21	DM48	DM48	M24	DM48
F22	DM49	DM49	M25	DM49
F23	DM50	DM50	M27	DM50
F24	DM51	DM51	M26	DM51
A3	DM52	DM52	M28	DM52
F18	DM53	DM53	M22	DM53
D15	DM54	DM54	M25	DM54
D17	DM55	DM55	M24	DM55
A4	DM56	DM56	M26	DM56
F21	DM57	DM57	M27	DM57
B1	DM58	DM58	M28	DM58
C12	DM59	DM59	M24	DM59
C13	DM60	DM60	M25	DM60
D20	DM61	DM61	M22	DM61
D19	DM62	DM62	M25	DM62
B10	DM63	DM63	M24	DM63
A2	DM64	DM64	M26	DM64
B3	DM65	DM65	M28	DM65
F21	DM66	DM66	M24	DM66
F22	DM67	DM67	M25	DM67
F23	DM68	DM68	M27	DM68
F24	DM69	DM69	M26	DM69
A3	DM70	DM70	M28	DM70
F18	DM71	DM71	M22	DM71
D15	DM72	DM72	M25	DM72
D17	DM73	DM73	M24	DM73
A4	DM74	DM74	M26	DM74
F21	DM75	DM75	M27	DM75
B1	DM76	DM76	M28	DM76
C12	DM77	DM77	M24	DM77
C13	DM78	DM78	M25	DM78
D20	DM79	DM79	M22	DM79
D19	DM80	DM80	M25	DM80
B10	DM81	DM81	M24	DM81
A2	DM82	DM82	M26	DM82
B3	DM83	DM83	M28	DM83
F21	DM84	DM84	M24	DM84
F22	DM85	DM85	M25	DM85
F23	DM86	DM86	M27	DM86
F24	DM87	DM87	M26	DM87
A3	DM88	DM88	M28	DM88
F18	DM89	DM89	M22	DM89
D15	DM90	DM90	M25	DM90

MPC8536  
GROUND  
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W1\_PFC-RFF 0



## MPC8536 DECOUPLING



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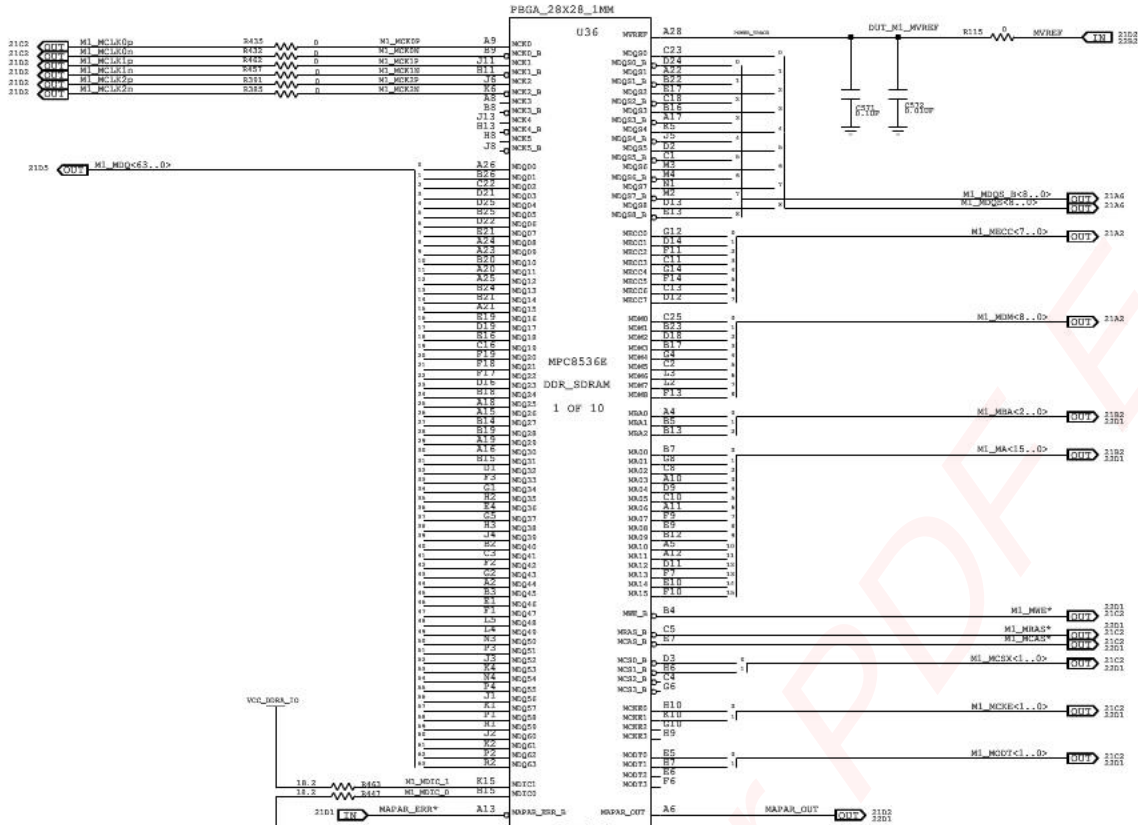
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# MPC8536 DDR CHANNEL



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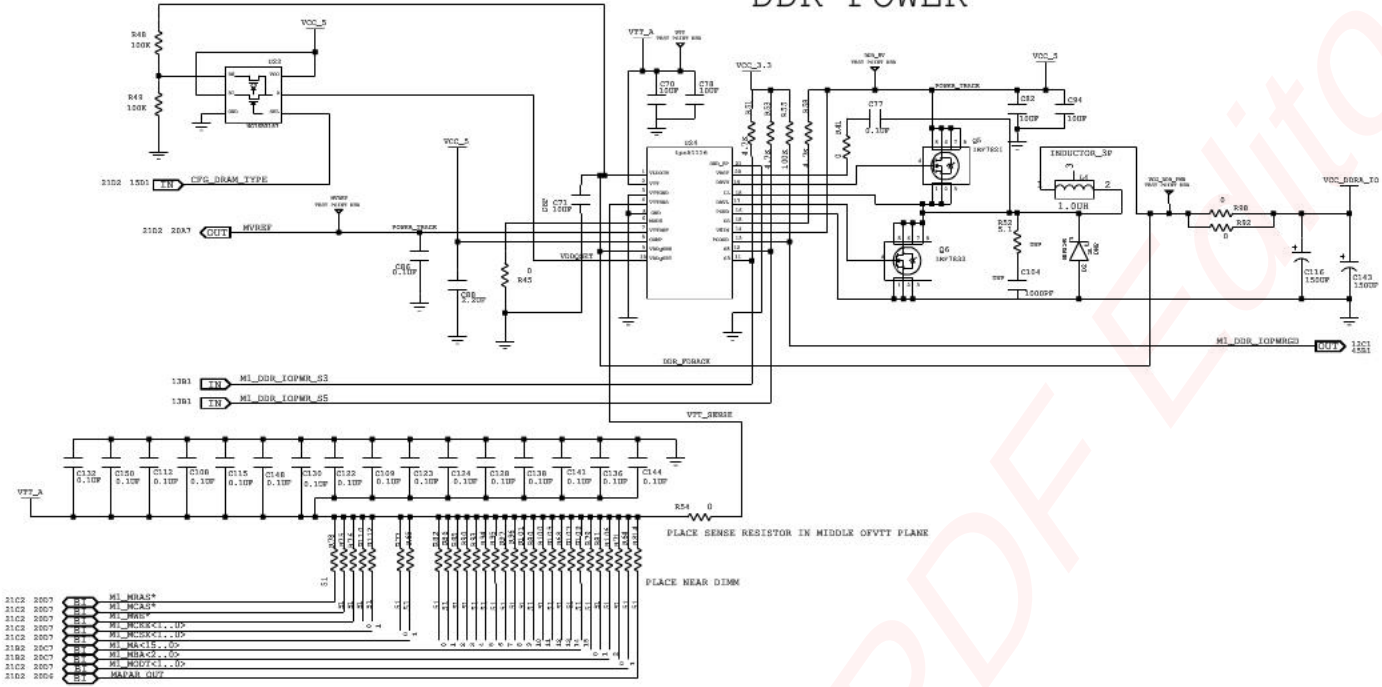
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# DDR POWER



# DDR TERMINATION

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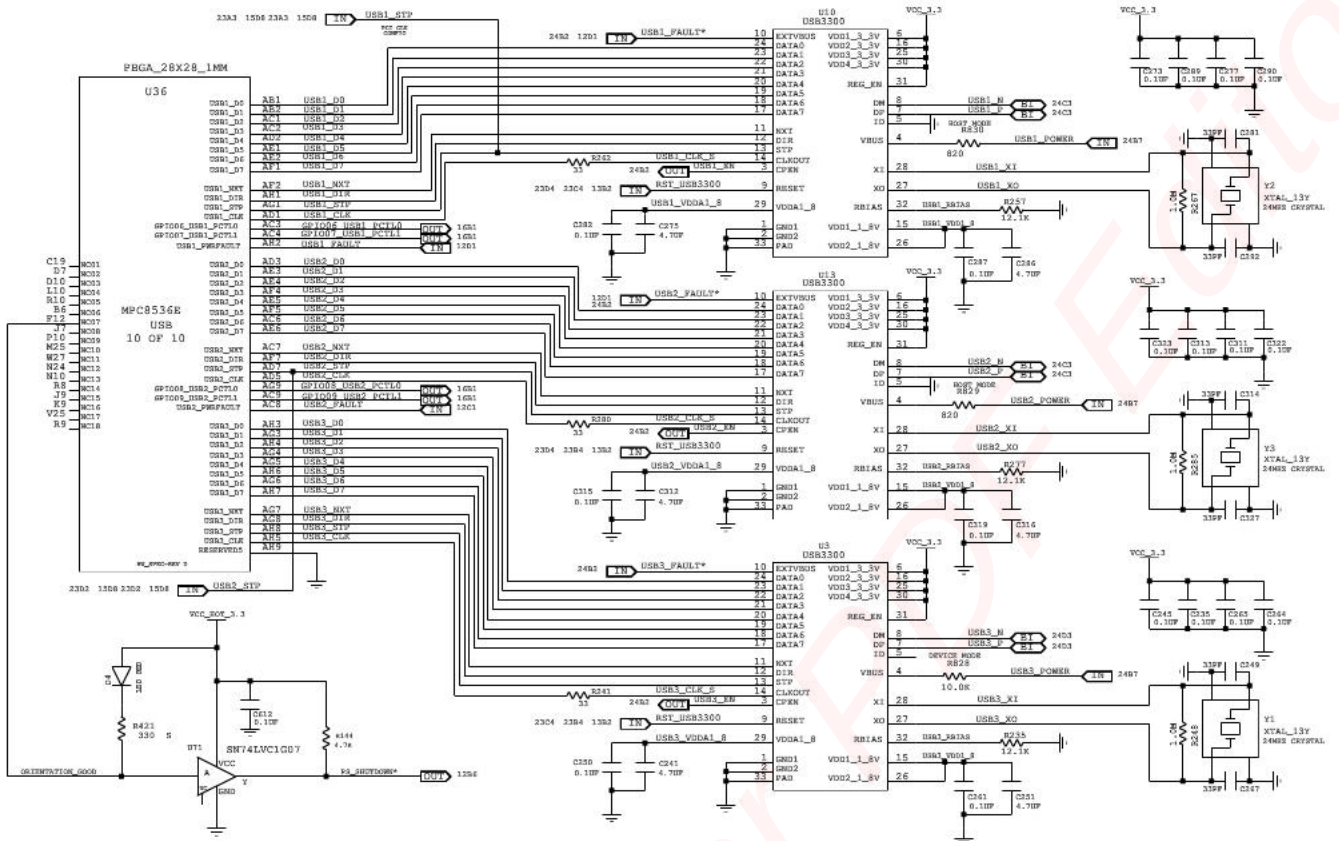
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# MPC8536 USB AND PHYS



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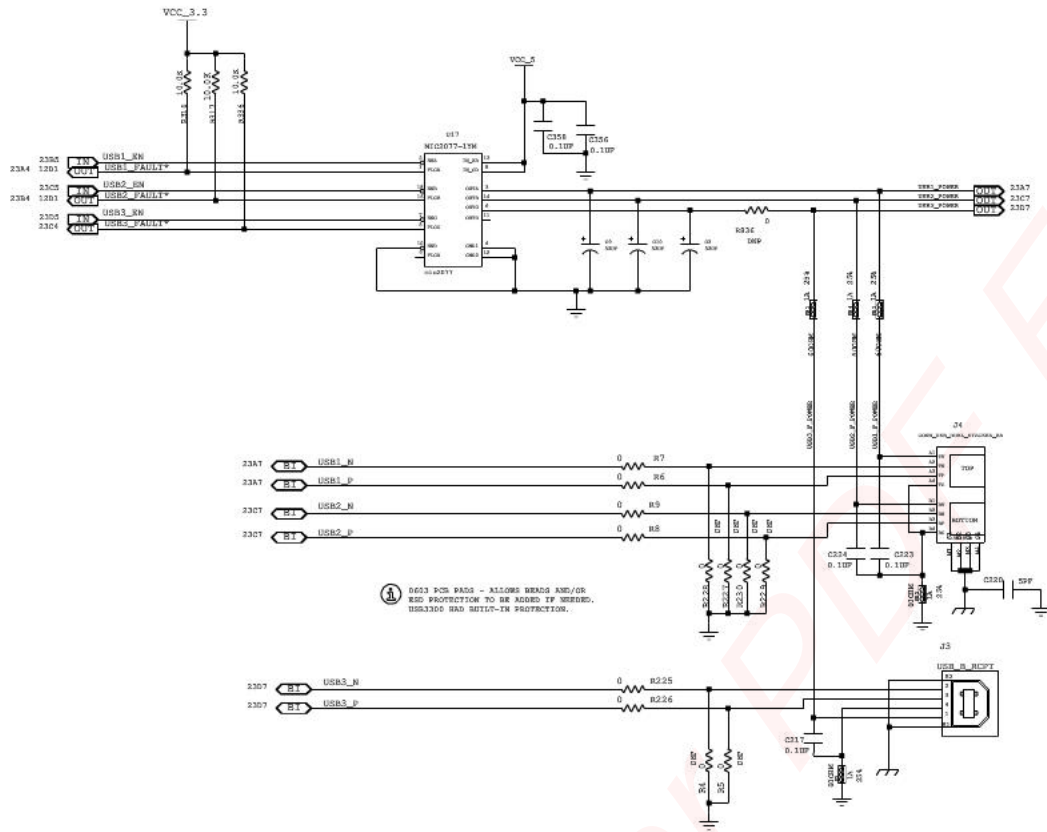
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# USB PORTS AND POWER



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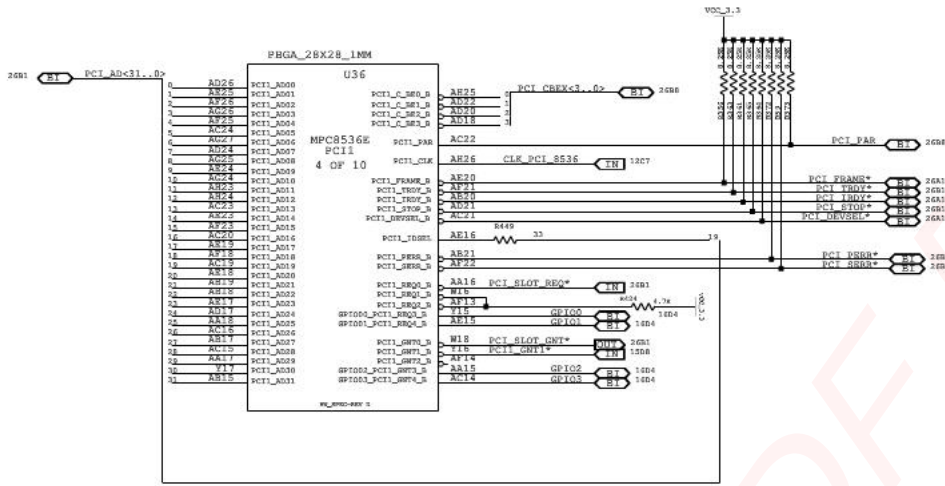
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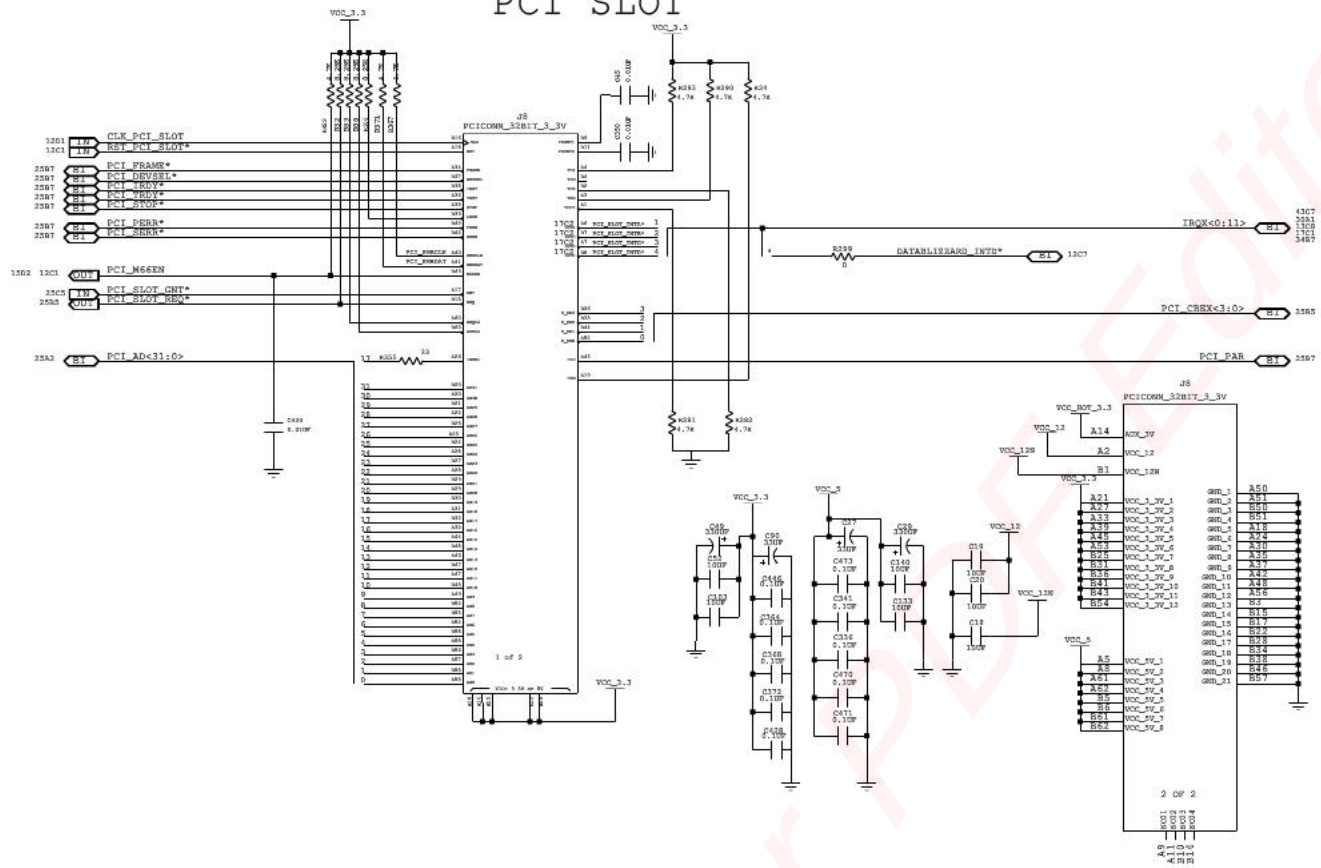
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# MPC8536 PCI



# PCI SLOT



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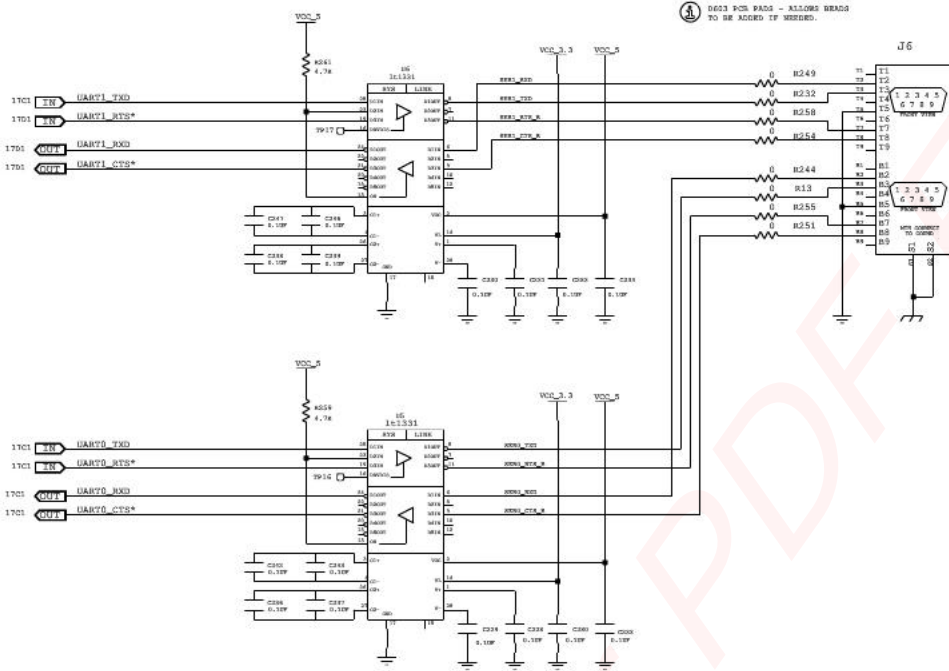
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# SERIAL PORTS 1 AND 2



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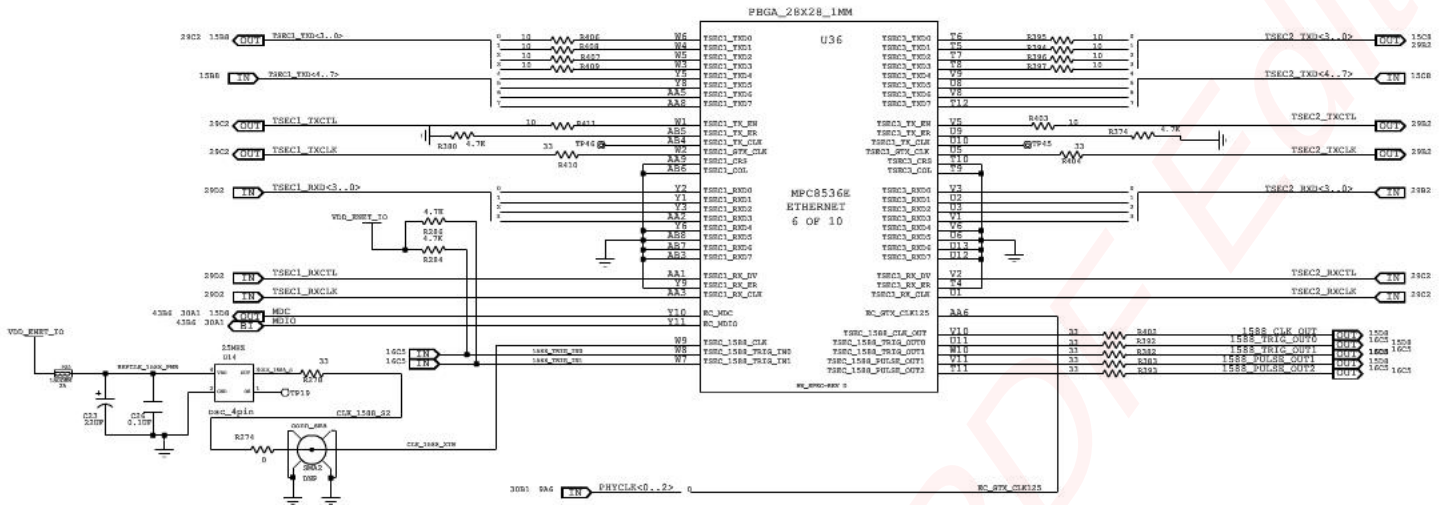
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# MPC8536 ETHERNET- RGMII



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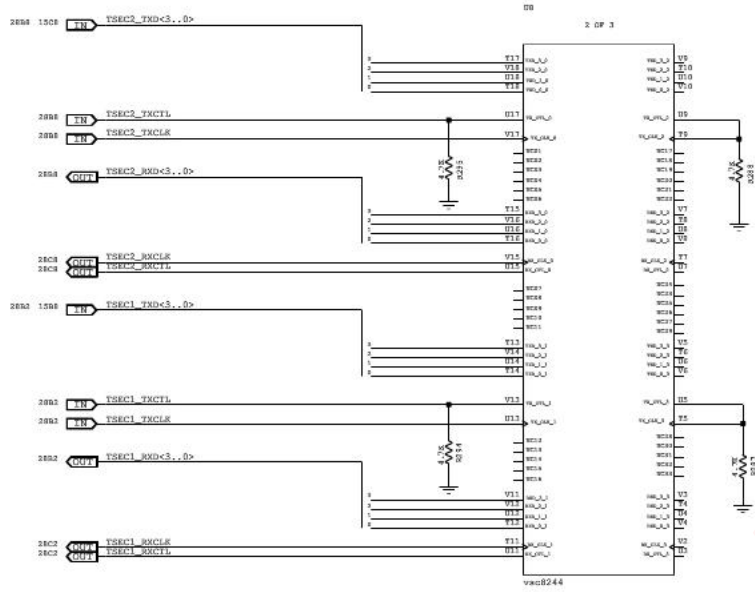
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VITESSE PHY 1 OF 3



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DATE: Fri Aug 01 13:51:45 2008

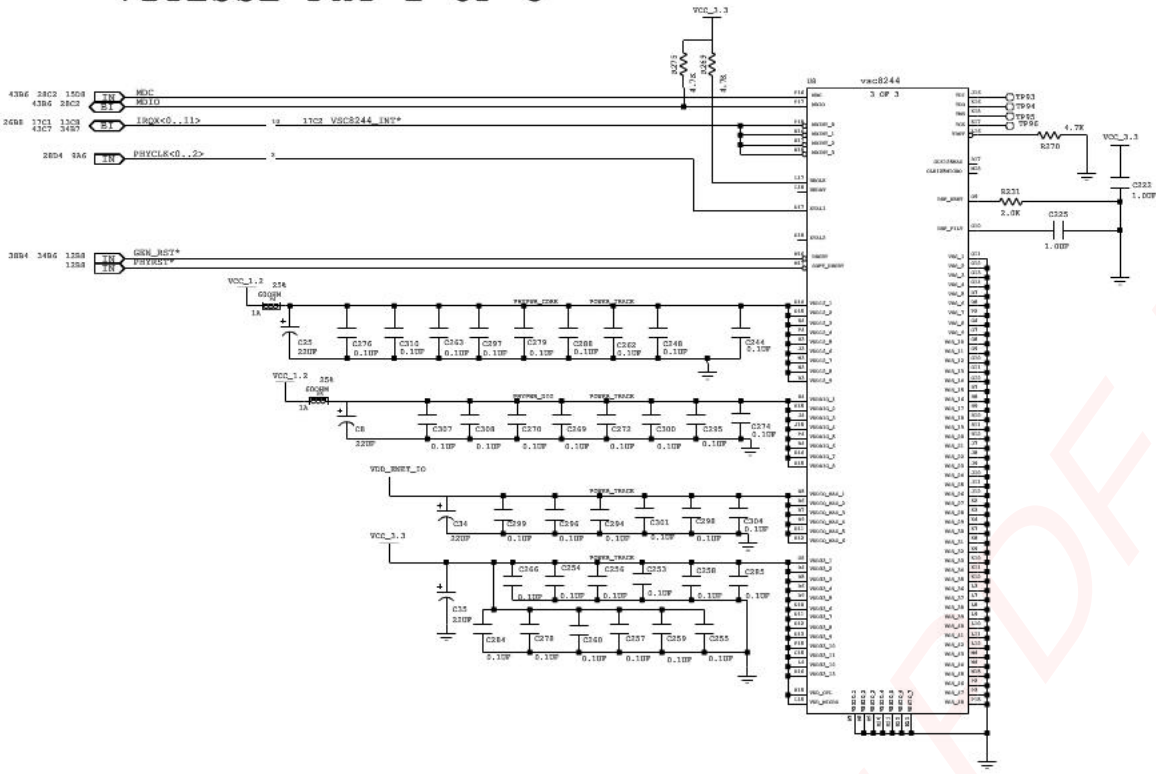
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# VITESSE PHY 2 OF 3



FREESCALE

DATE: Fri Aug 01 13:52:01 2008

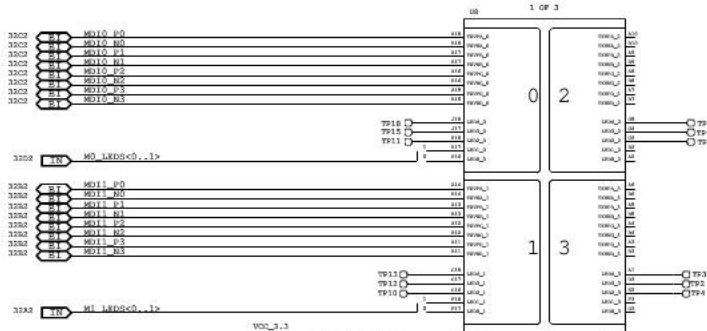
PROJECT: CALAMARI

ENGINEER: MICHAEL GEORGE

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1	2	3	4	5	6	7	8
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Clock	Pin	Definition	Value	Ref	Resistance
0	0	MDIO_00	0		
0	1	MDIO_01	0		
0	2	MDIO_02	0	3100	8.20K -> 8.20K
0	3	MDIO_03	0		
0	4	MDIO_04	0		
0	5	MDIO_05	0		
1	0	MII_00	0		
1	1	MII_01	0		
1	2	MII_02	0	3100	8.20K -> 8.20K
1	3	MII_03	0		
1	4	MII_04	0		
1	5	MII_05	0		
2	0	MDIO_00	0		
2	1	MDIO_01	0	3100	8 -> 8.20K
2	2	MDIO_02	0		
2	3	MDIO_03	0		
2	4	MDIO_04	0		
2	5	MDIO_05	0		
3	0	MII_00	0		
3	1	MII_01	0	3100	8 -> 8.20K
3	2	MII_02	0		
3	3	MII_03	0		
3	4	MII_04	0		
3	5	MII_05	0		
4	0	MDIO_00	0		
4	1	MDIO_01	0	3100	8 -> 8.20K
4	2	MDIO_02	0		
4	3	MDIO_03	0		
4	4	MDIO_04	0		
4	5	MDIO_05	0		
5	0	MII_00	0		
5	1	MII_01	0	3100	8.20K -> 8.20K
5	2	MII_02	0		
5	3	MII_03	0		
5	4	MII_04	0		
5	5	MII_05	0		
6	0	MDIO_00	0		
6	1	MDIO_01	0	3100	8.20K -> 8.20K
6	2	MDIO_02	0		
6	3	MDIO_03	0		
6	4	MDIO_04	0		
6	5	MDIO_05	0		
7	0	MII_00	0		
7	1	MII_01	0	3100	8.20K -> 8.20K
7	2	MII_02	0		
7	3	MII_03	0		
7	4	MII_04	0		
7	5	MII_05	0		



NOTE: SGM11-ID mode of VDCB244 used to implement both TX/RX clock delays in lieu of routing restrictions.

FREESCALE

DATE: Fri Aug 01 13:52:17 2008

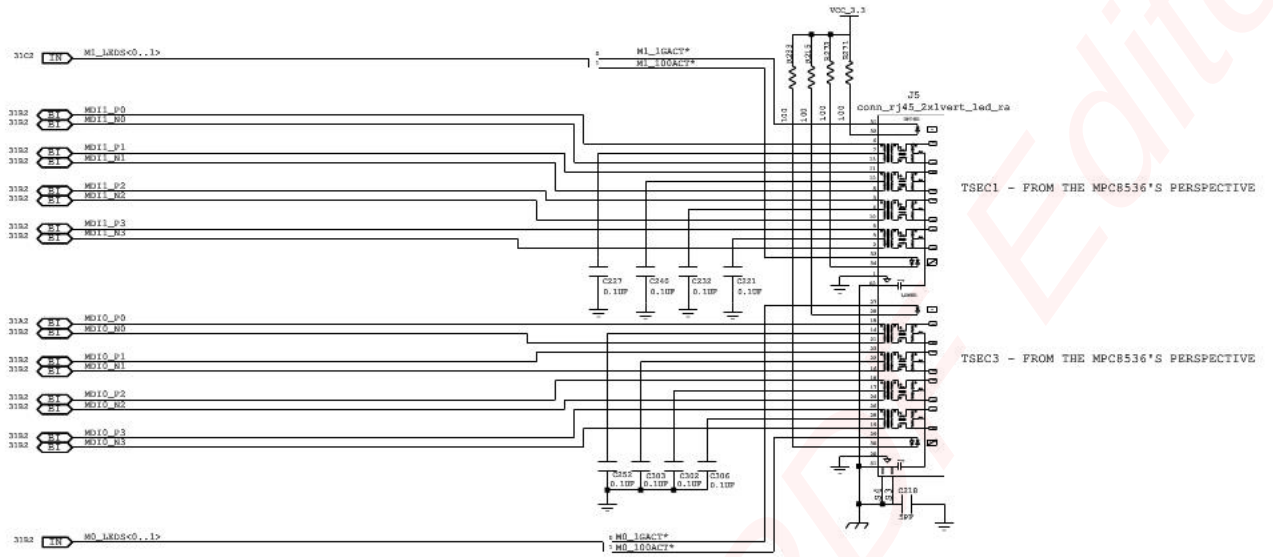
PROJECT: CALAMARI

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# ETHERNET PORT CONNECTORS



FREESCALE

DATE: Fri Aug 01 13:52:33 2008

PROJECT: CALAMARI

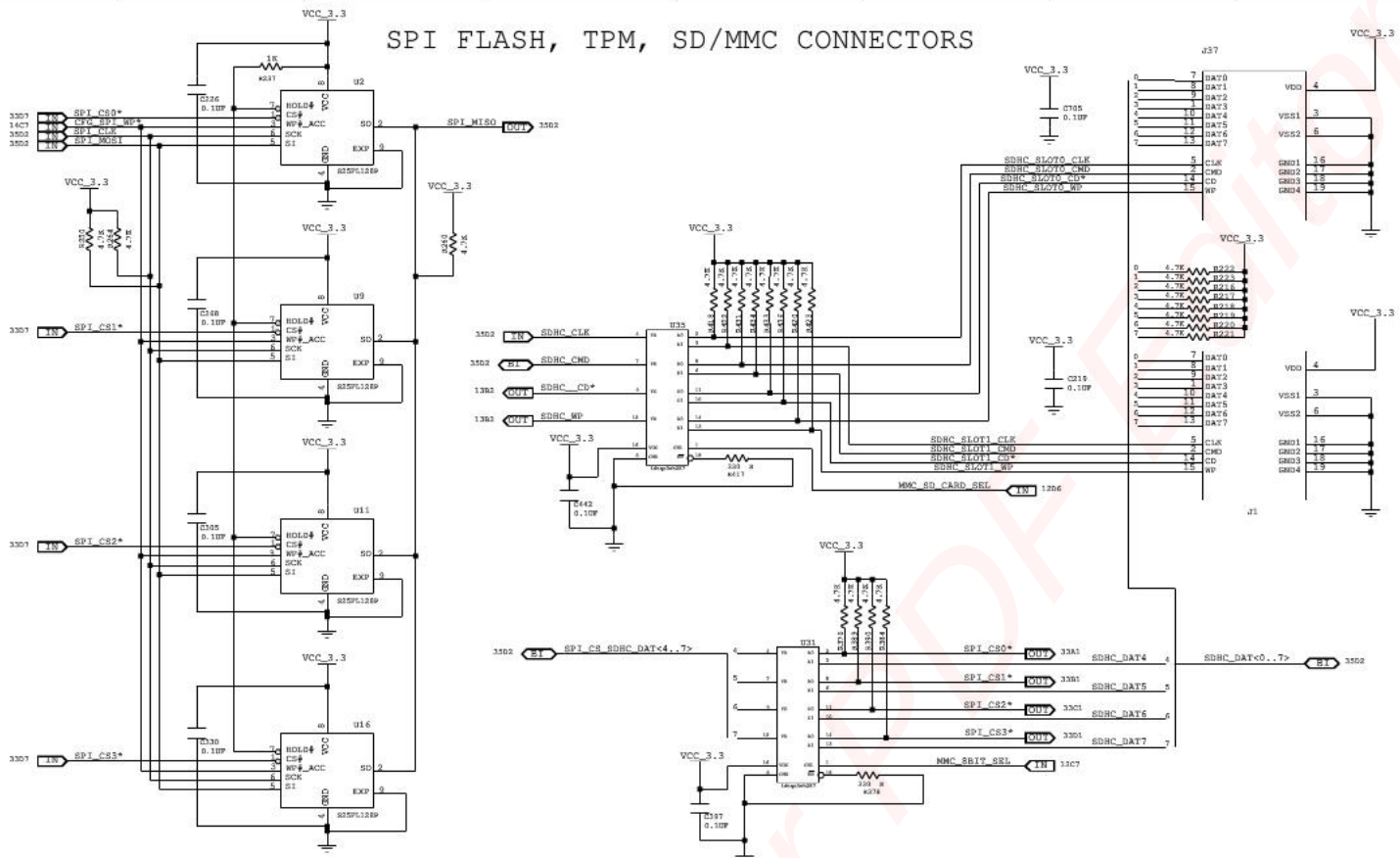
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# SPI FLASH, TPM, SD/MMC CONNECTORS



FREESCALE

DATE: Fri Aug 01 13:52:52 2008

PROJECT: CALAMARI

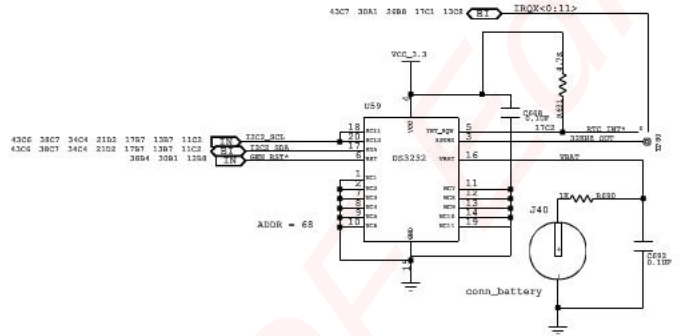
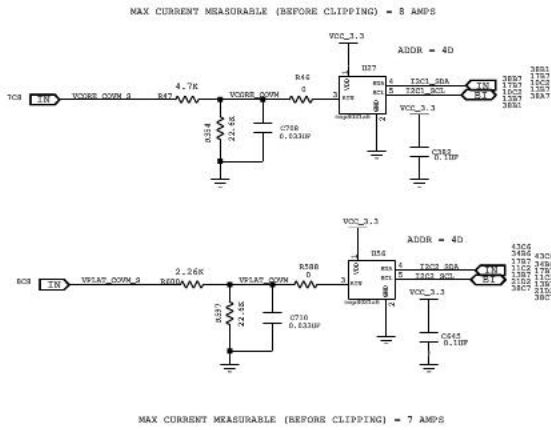
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# RTC/NVRAM WITH BATTERY, I2C A/D'S



FREESCALE

DATE: Fri Aug 01 13:53:12 2008

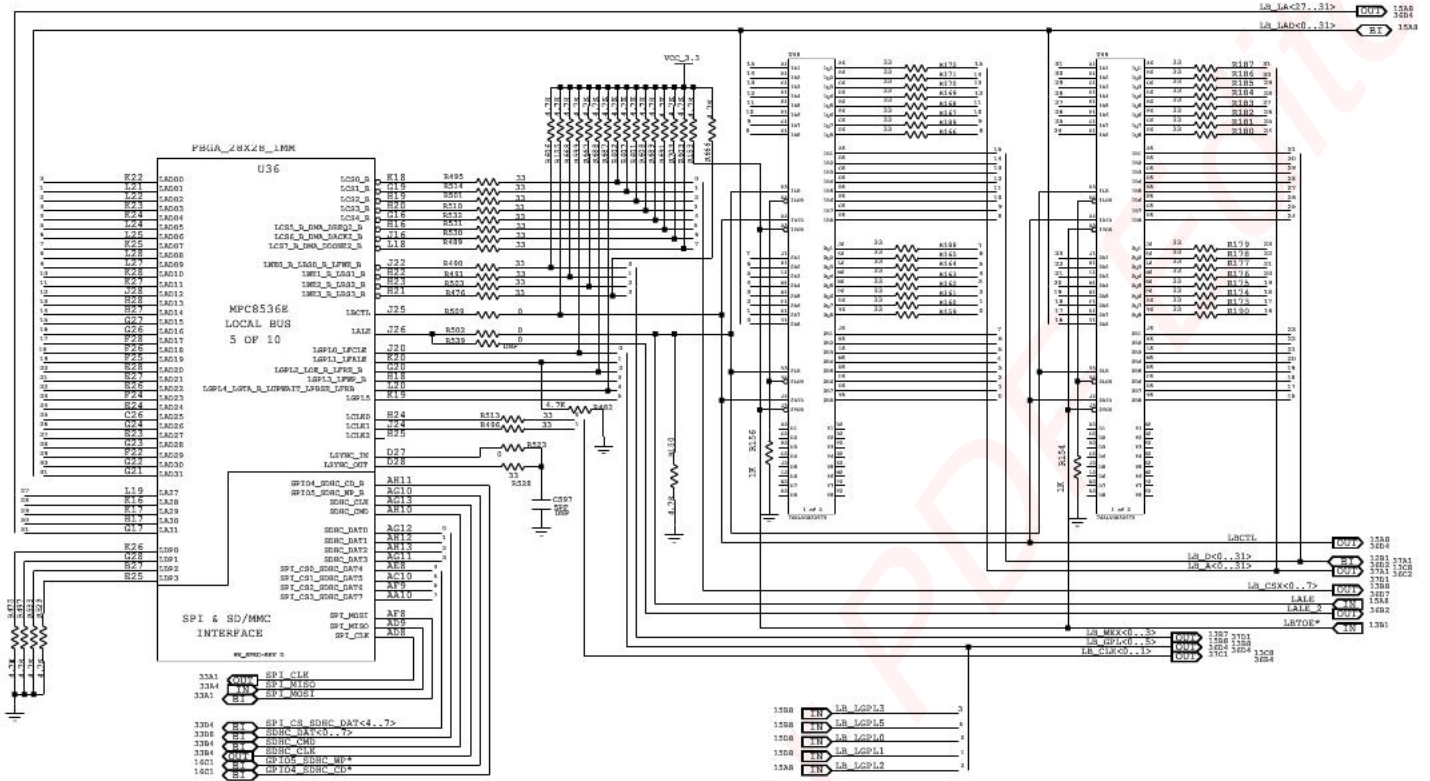
PROJECT: CALAMARI

ENGINEER: MICHAEL GEORGE

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# MPC8536 LOCAL BUS, SPI, SD INTERFACES



FREESCALE

DATE: Fri Aug 01 13:53:30 2008

PROJECT: CALAMARI

ENGINEER: MICHAEL GEORGE

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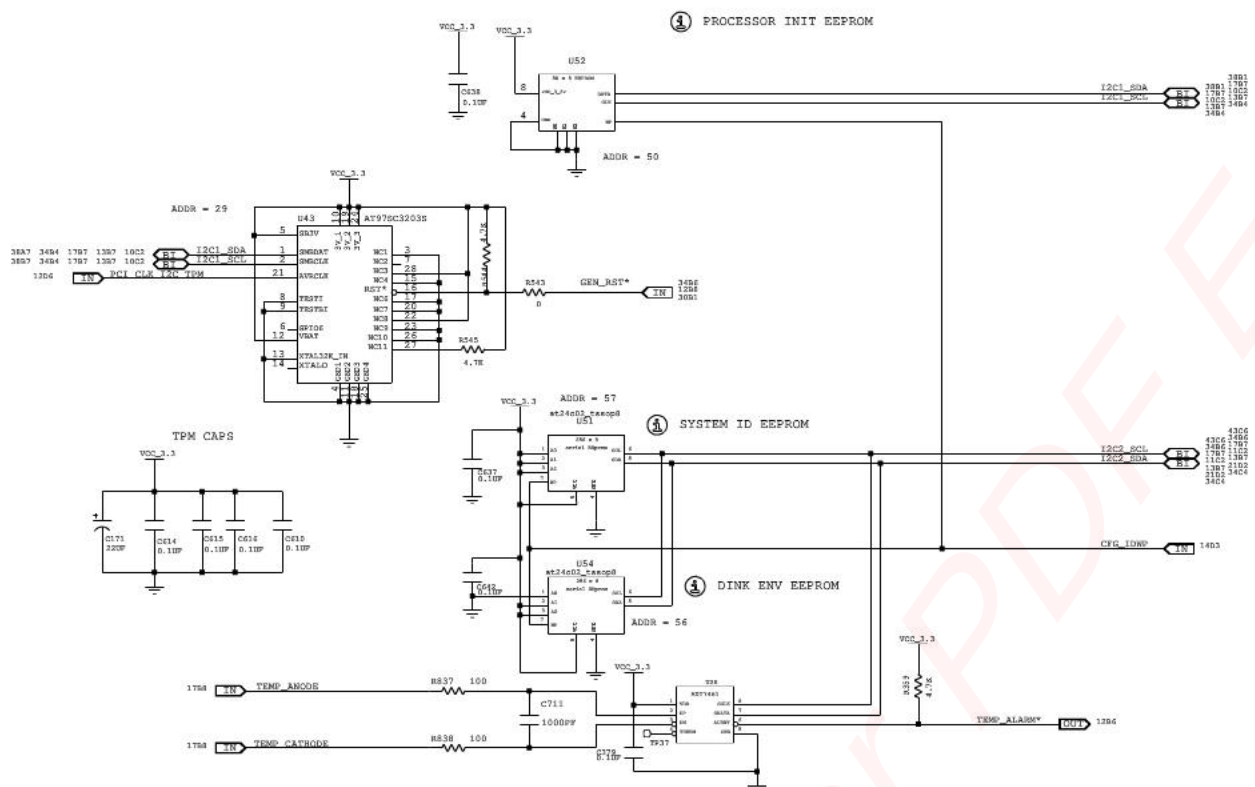
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# I2C DEVICES



FREESCALE

DATE: Fri Aug 01 13:54:32 2008

PROJECT: CALAMARI

ENGINEER: MICHAEL GEORGE

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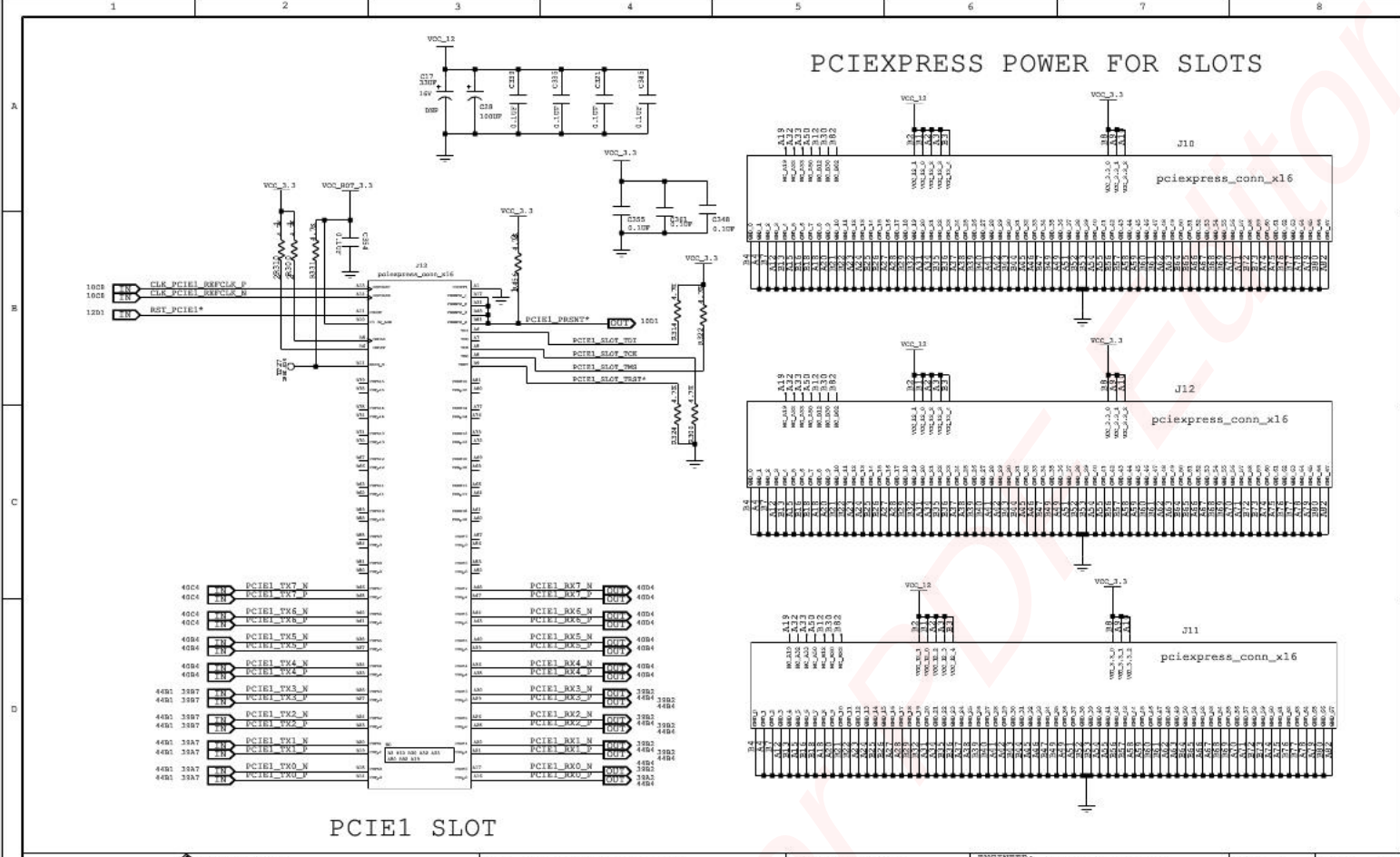
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PCI E1 SLOT

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PROJECT: CALAMARI

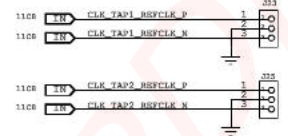
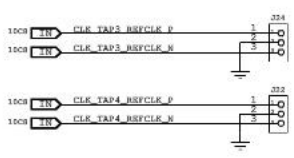
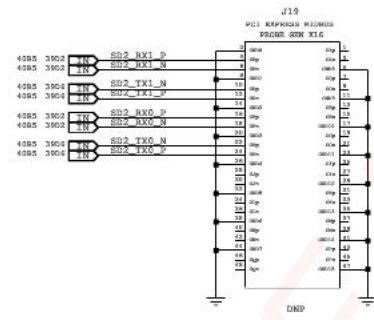
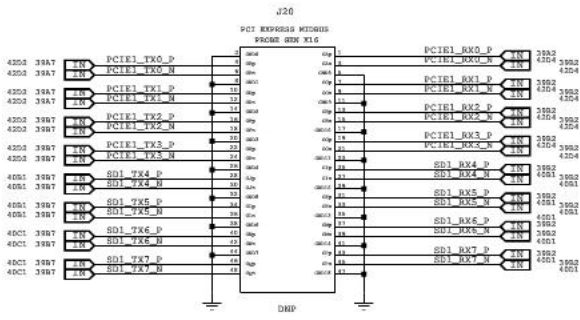
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# MIDBUS PROBE



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DATE: Fri Aug 01 13:55:59 2008

PROJECT: CALAMARI

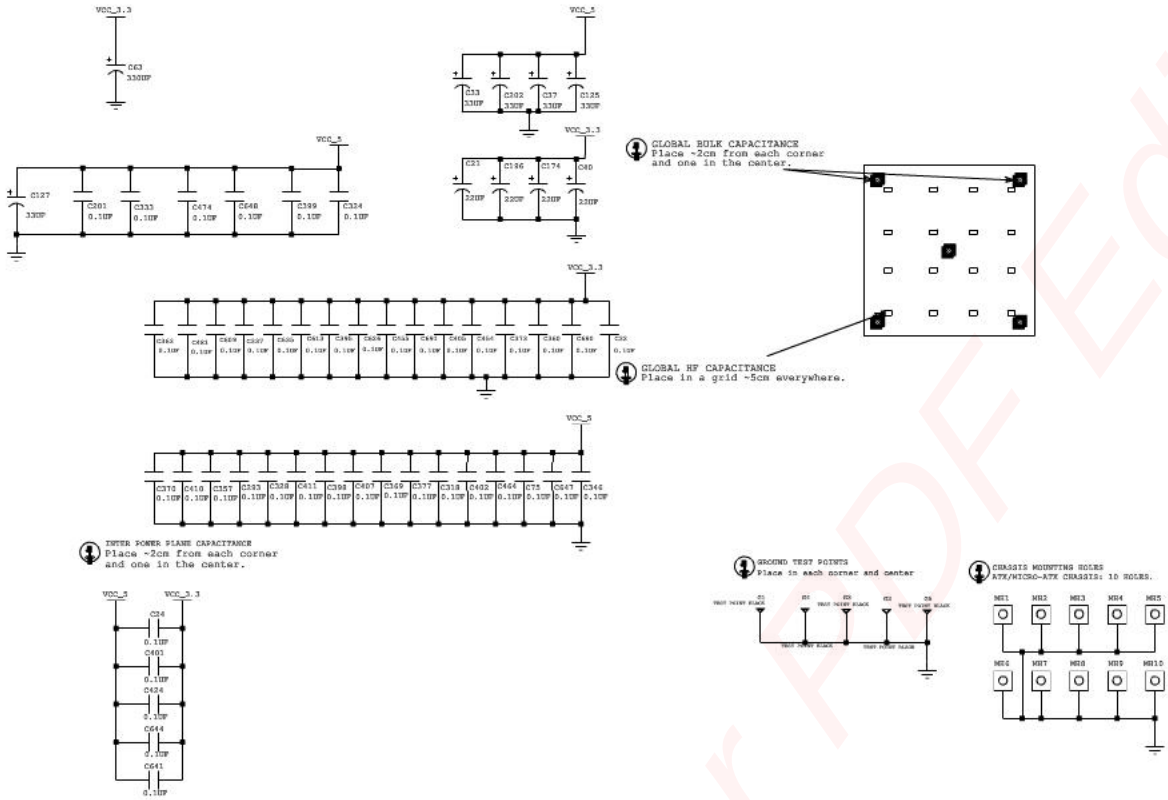
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# GLOBAL BYPASS, MOUNTING, ETC



FREESCALE

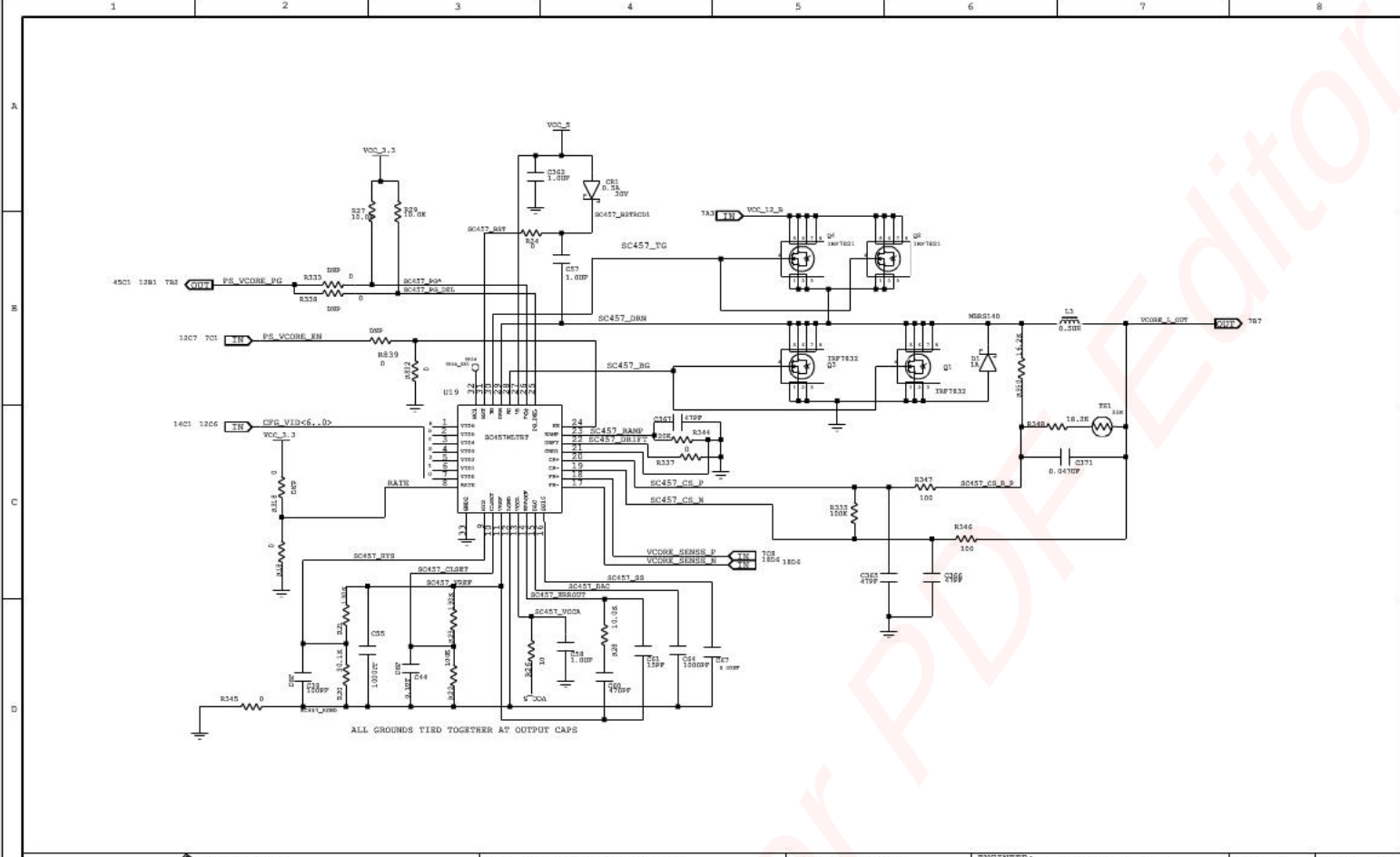
DATE: Fri Aug 01 13:56:34 2008

PROJECT: CALAMARI

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FREESCALE

DATE: Fri Aug 01 13:56:49 2008

PROJECT: CALAMARI

ENGINEER: MICHAEL GEORGE

REV: B.1

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