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CUSIIC

MPC8536 DEVELOPMENT PLATFORM
CALAMARI

FREESCALE	DATE: Fri Aug 01 13:44:45 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 1 OF 47

GENERAL INFORMATION

PAGE	CONTENTS
01	COVER PAGE
02	GENERAL INFORMATION
03	BLOCK DIAGRAM
04	PCB STACKUP
05	ATX POWER ENTRY, RESET SWITCHES
06	HOT POWER SUPPIES (3.3V, 2.5V, 1.5V)
07	VCC CORE SUPPLY (PRIMARY OPTION)
08	VPLAT POWER AND 1.2V POWER
09	CLOCK GENERATION - SYSCLK, DDR & ETHERNET
10	SERDES1 CLOCK GENERATION
11	SERDES2 CLOCK GENERATION
12	FPGA SYSTEM LOGIC PART 1
13	FPGA SYSTEM LOGIC PART 2
14	CONFIGURATION SWITCHES
15	CONFIGURATION TRISTATE BUFFERS
16	COP, GPIO, AND 1588 HEADERS
17	MPC8536 MISC
18	MPC8536 POWER
19	MPC8536 GND AND DECOUPLING
20	MPC8536 DDR
21	DDR DIMM CONNECTOR
22	DDR POWER AND TERMINATION RESISTORS
23	MPC8536 USB AND PHYS
24	USB PORTS AND POWER
25	MPC8536 PCI
26	PCI SLOT
27	SERIAL PORTS #1 AND #2
28	MPC8536 ETHERNET
29	VITESSE PHY 1 OF 3
30	VITESSE PHY 2 OF 3
31	VITESSE PHY 3 OF 3
32	ETHERNET PORT CONNECTORS #1/#2
33	SPI FLASH, TPM, AND SD/MMC CONNECTORS
34	RTC/NVRAM WITH BATTERY, I2C A/D'S
35	MPC8536 LOCAL BUS
36	LOCAL BUS VISIBILITY, LATCH POWER
37	NOR, NAND FLASH, PROMJET HEADER
38	I2C DEVICES
39	MPC8536 SERDES
40	HIGH SPEED MUXES AND SATA CONNECTORS
41	PCIEXPRESS SLOT #2 & #3
42	PCIEXPRESS SLOT #1, AND POWER FOR SLOTS
43	SGMII CONNECTOR
44	MIDBUS PROBE
45	DEBUG LEDS
46	GLOBAL BPASS, MOUNTING, ETC
47	VCC VCORE SC457 (LAB USE ONLY)

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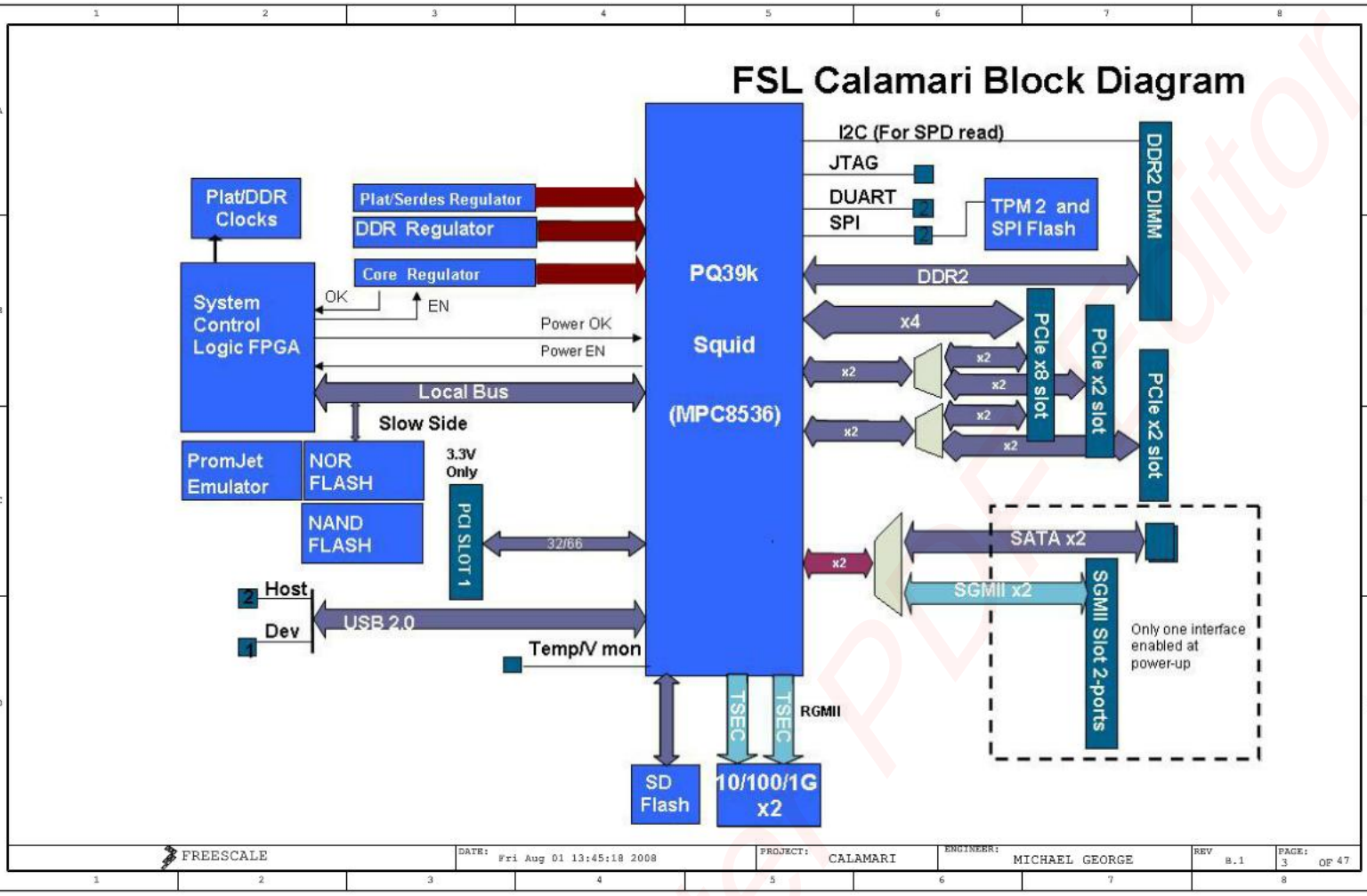
SCHEMATIC HISTORY

B.0	INITIAL VERSION FOR RE-SPIN
B.0	CORRECTS ALL KNOWN ERRATA (CE1-CE5)
B.0	ADDED VBUS PROTECTION RESISTORS
B.0	CONNECTED CONFIG_SYS(3) TO FPGA
B.0	ADDED TWO TESTPOINTS TO THE FPGA
B.0	DATABLIZZARD INTD MOVED FROM INTA TO INTD
B.0	ADDED ESATA SSD PROTECTION
B.0	VBUS POWER FOR USB#3 REMOVED FROM 2077
B.0	PCI_CLK CPG RAN THROUGH POR BUFFERS
B.0	REMOVED 1.5V LED
B.0	ADDED FILTER CAP & RESISTORS TO ADT7561
B.0	SEPARATED VCORE ENABLES
B.1	ADDED GROUND TO U134-PIN #9

FREESCALE	DATE: Fri Aug 01 13:44:58 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 2 OF 47



PCB STACKUP

Lay #	Thick (in)	Picture	Type Dk Df	Description	Drill Picture
0.0007/0.0007			3.20	Soldermask	
1	0.0022		F	1/2oz w/plating	1
	0.0040	1-2113	4.40 0.018	fill	
2	0.0013		P	1oz	2
	0.0080	2-2116	4.47 0.018	core	
3	0.0013		P	1oz	3
	0.0053	1-1652	4.47 0.018	fill	
4	0.0006		S	1/2oz	4
	0.0120	2-1506	4.49 0.018	core	
5	0.0006		S	1/2oz	5
	0.0053	1-1652	4.47 0.018	fill	
6	0.0013		P	1oz	6
	0.0080	2-2116	4.47 0.018	core	
7	0.0013		P	1oz	7
	0.0053	1-1652	4.47 0.018	fill	
8	0.0006		S	1/2oz	8
	0.0120	2-1506	4.49 0.018	core	
9	0.0006		S	1/2oz	9
	0.0053	1-1652	4.47 0.018	fill	
10	0.0013		P	1oz	10
	0.0080	2-2116	4.47 0.018	core	
11	0.0013		P	1oz	11
	0.0040	1-2113	4.40 0.018	fill	
12	0.0022		F	1/2oz w/plating	12
0.0007/0.0007			3.20	Soldermask	

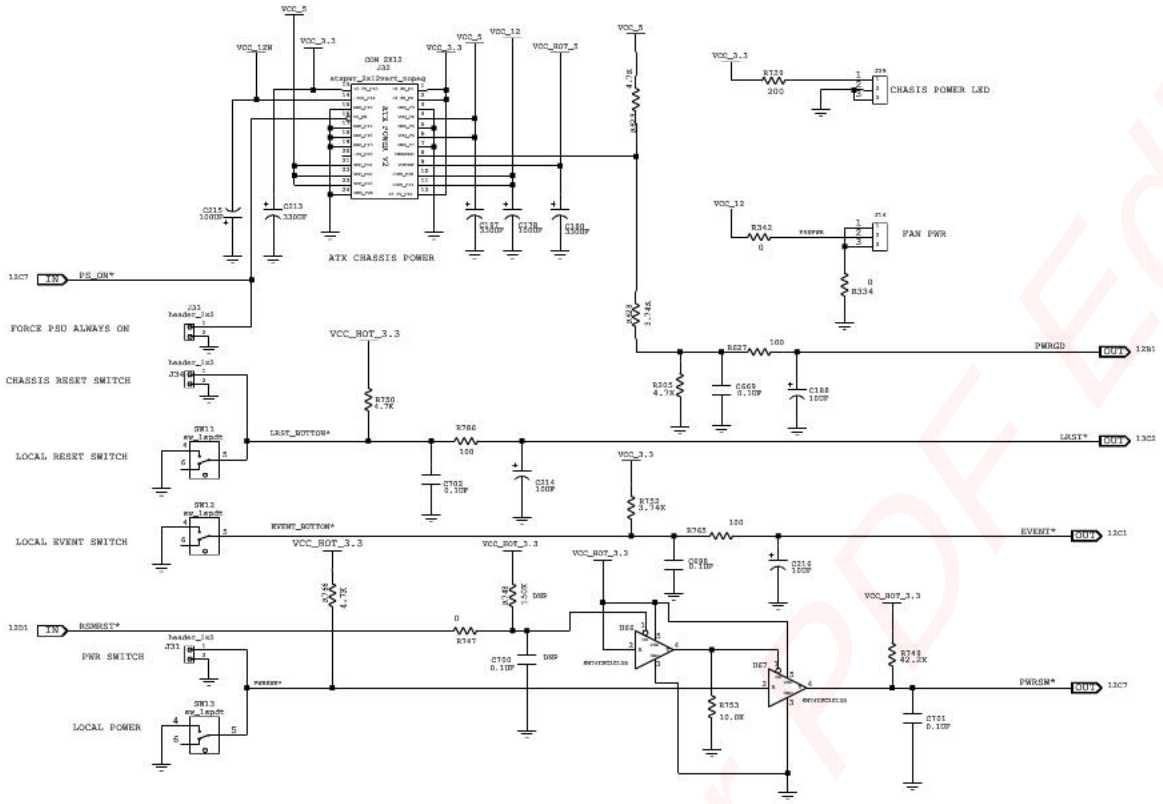
0.0927	Total thickness (in) Over metal(with solder mask)
0.0881	After lamination thickness (in)
0.0883	Over laminate thickness (in) (with soldermask)
0.0930	Customer Requirement (in)
+/-0.0090	Customer Tolerance (in)

Impedance Constraint Information

Imp #	Imp Type Name	Picture	Affect Lur (1)	(2)	Line Width (1)	(2)	Center-to-Center (1)	(2)	Ref Plane Top	Bot	Targ ohms	Tol ohms	tpd ps/in	Atten dB/in	Predict ohms
1	Surf MS		1	None	0.005				None	2	55	5	153	0.24	54.41
2	Surf MS		1	None	0.006				None	2	50	5	154	0.23	50.00
3	EC MS		1	None	0.0045	0.0045	0.0115		None	2	100	10	153	0.24	99.76
4	Stripline		4	None	0.006				3	6	50	5.5	179	0.28	51.41
5	Stripline		4	None	0.005				3	6	55	5.5	179	0.28	55.85
6	EC SL		4	None	0.004	0.004	0.008		3	6	100	10	184	0.30	93.90
7	EC SL		4	None	0.005	0.005	0.0125		3	6	100	10	181	0.29	98.35
8	Stripline		5	None	0.005				3	6	55	5.5	179	0.28	55.85
9	Stripline		5	None	0.006				3	6	50	5	179	0.28	51.41
10	EC SL		5	None	0.004	0.004	0.008		3	6	100	10	184	0.30	93.90
11	EC SL		5	None	0.005	0.005	0.0125		3	6	100	10	181	0.29	98.35
12	Stripline		8	None	0.006				7	10	50	5	179	0.28	51.41
13	Stripline		8	None	0.005				7	10	55	5.5	179	0.28	55.85
14	EC SL		8	None	0.004	0.004	0.008		7	10	100	10	184	0.30	93.90
15	EC SL		8	None	0.005	0.005	0.0125		7	10	100	10	181	0.29	98.35
16	Stripline		9	None	0.006				7	10	50	5	179	0.28	51.41
17	Stripline		9	None	0.005				7	10	55	5.5	179	0.28	55.85
18	EC SL		9	None	0.004	0.004	0.008		7	10	100	10	184	0.30	93.90
19	EC SL		9	None	0.005	0.005	0.0125		7	10	100	10	181	0.29	98.35
20	Surf MS		12	None	0.005				None	11	55	5	153	0.24	54.41
21	Surf MS		12	None	0.006				None	11	50	5	154	0.23	50.00
22	EC MS		12	None	0.0045	0.0045	0.0115		None	11	100	10	153	0.24	99.76

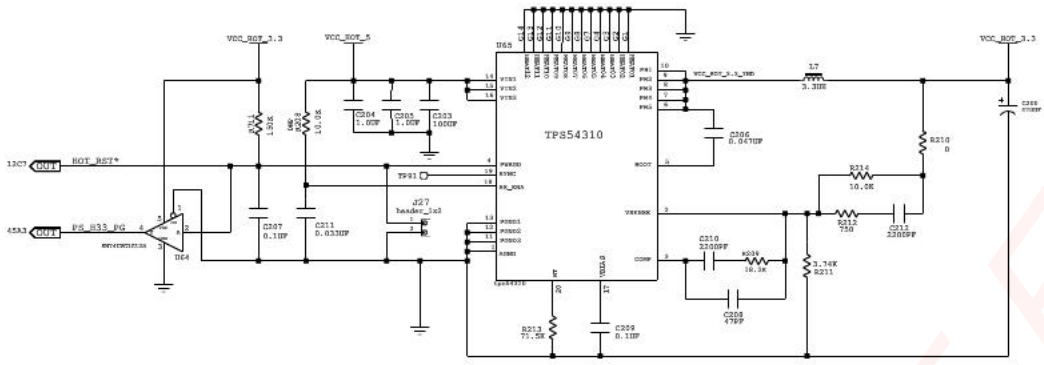
FREESCALE	DATE: Fri Aug 01 13:45:32 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 4 OF 47

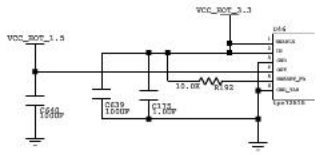
POWER ENTRY, USER SWITCHES

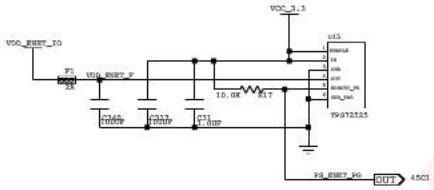


FREESCALE	DATE: Fri Aug 01 13:45:44 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 5 OF 47

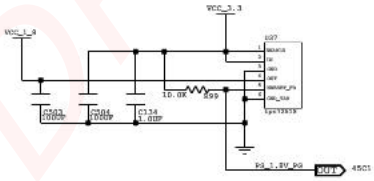
HOT POWER SUPPIES







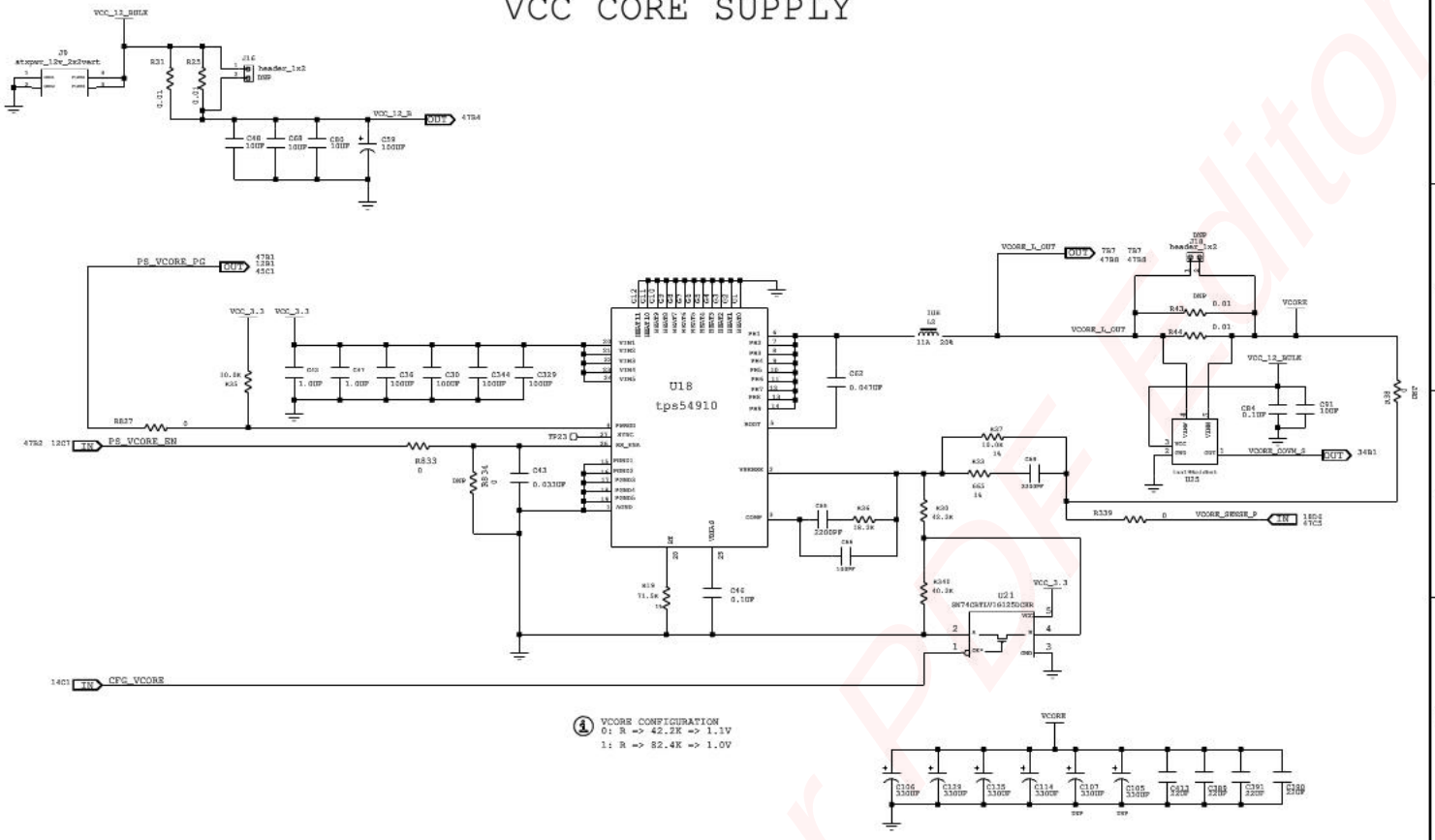
WORST CASE I/O < 1.5W (P=1.0A*2.5V).
COPPER AREA = 1 CM SQ



POWERS ONLY THE PCIE SIGNAL SWITCHES (..LESS THAN 30MW)
AS SUCH, ONLY THE BARE MINIMUM PCB COPPER AREA IS NEEDED.

FREESCALE	DATE: Fri Aug 01 13:45:59 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 6 OF 47

VCC CORE SUPPLY



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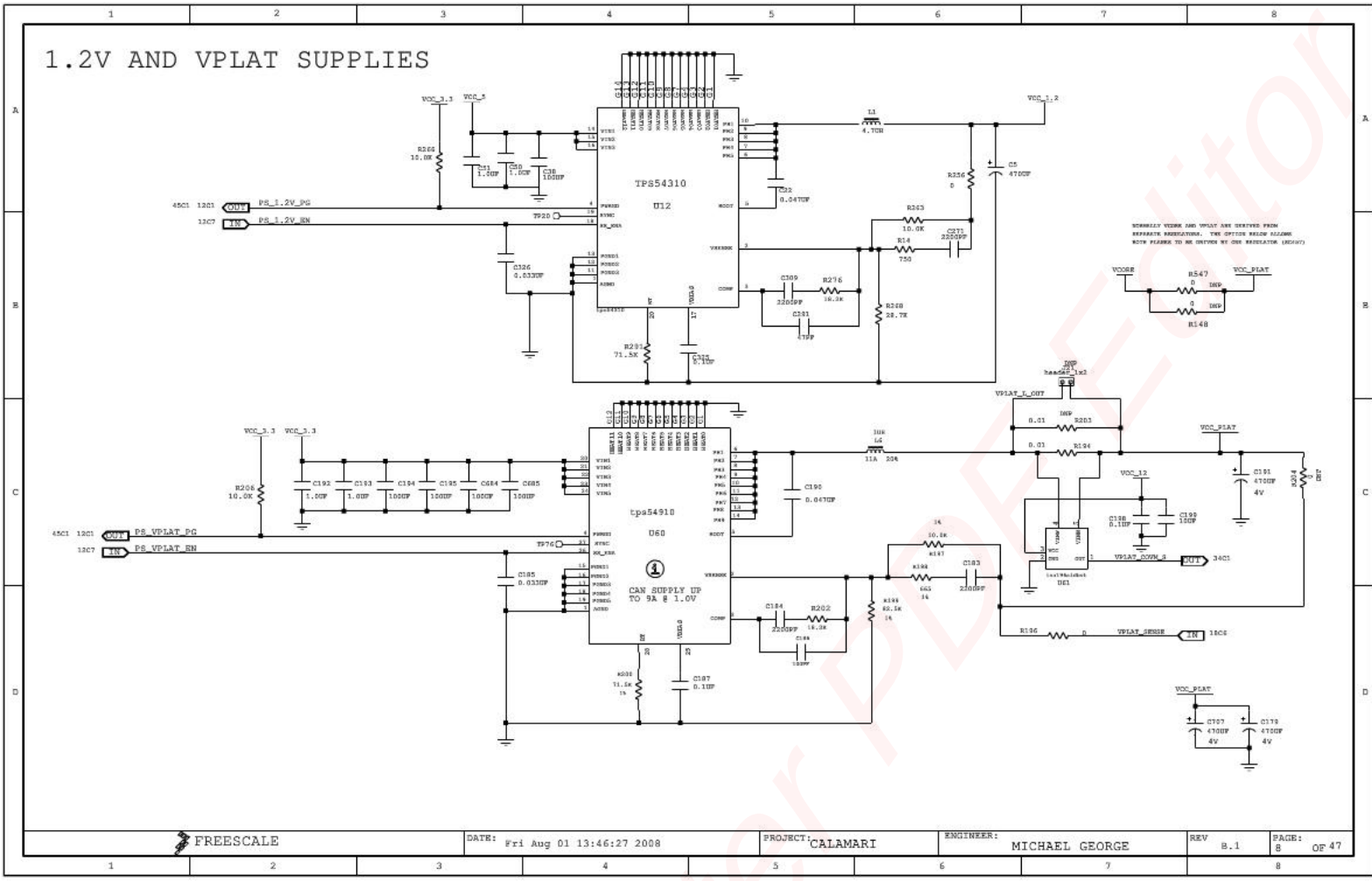
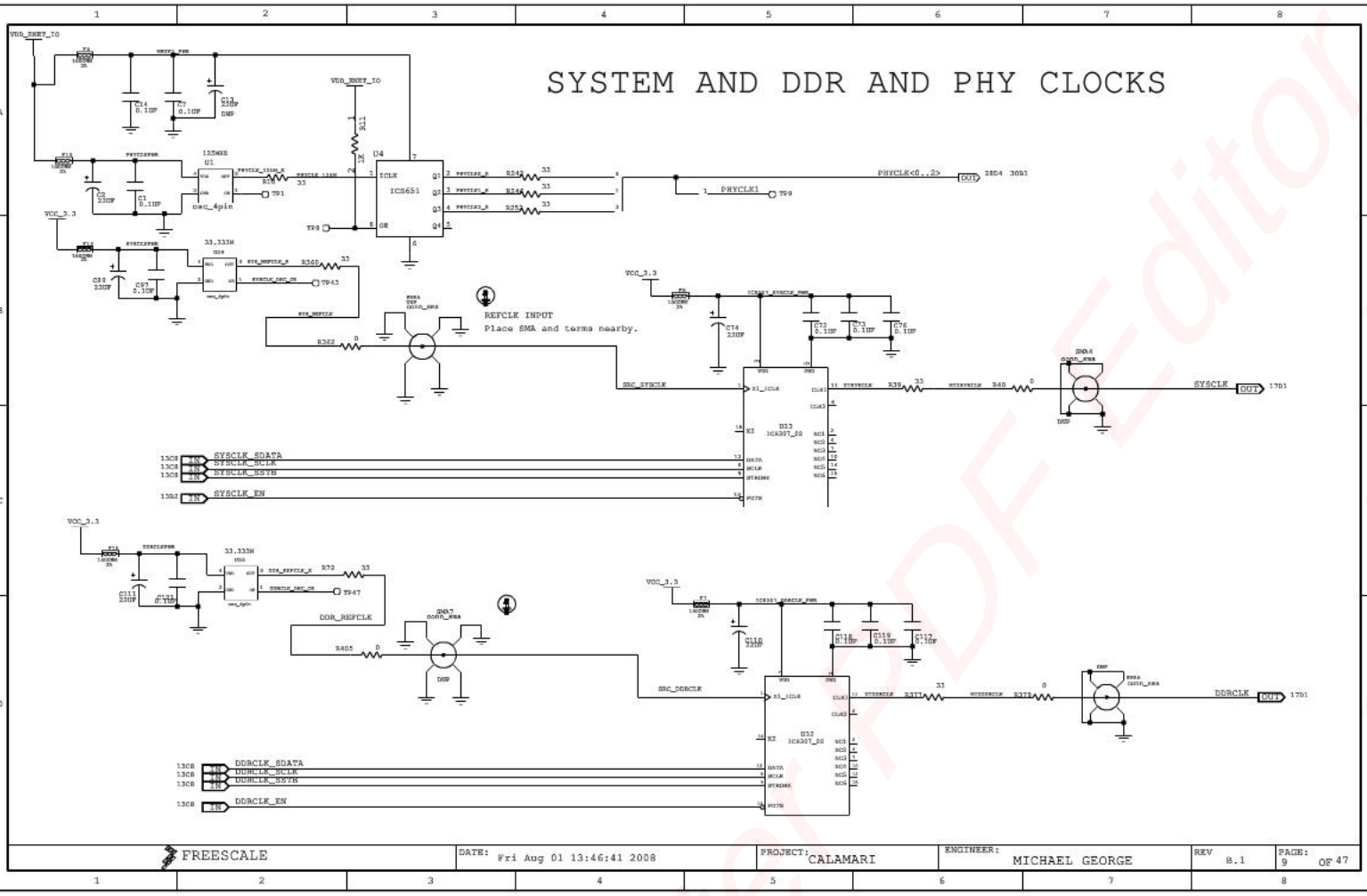
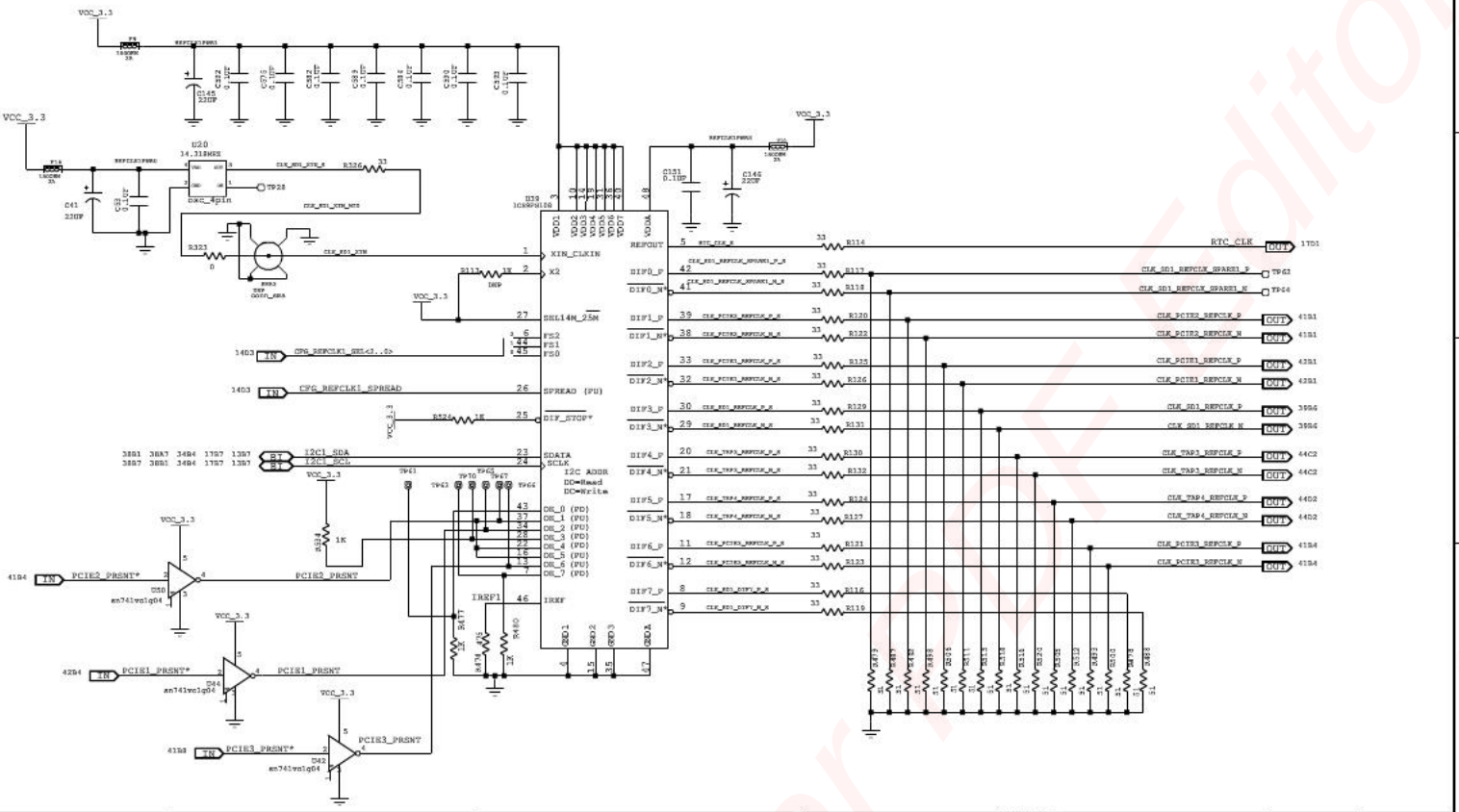




SERDES 1 CLOCK



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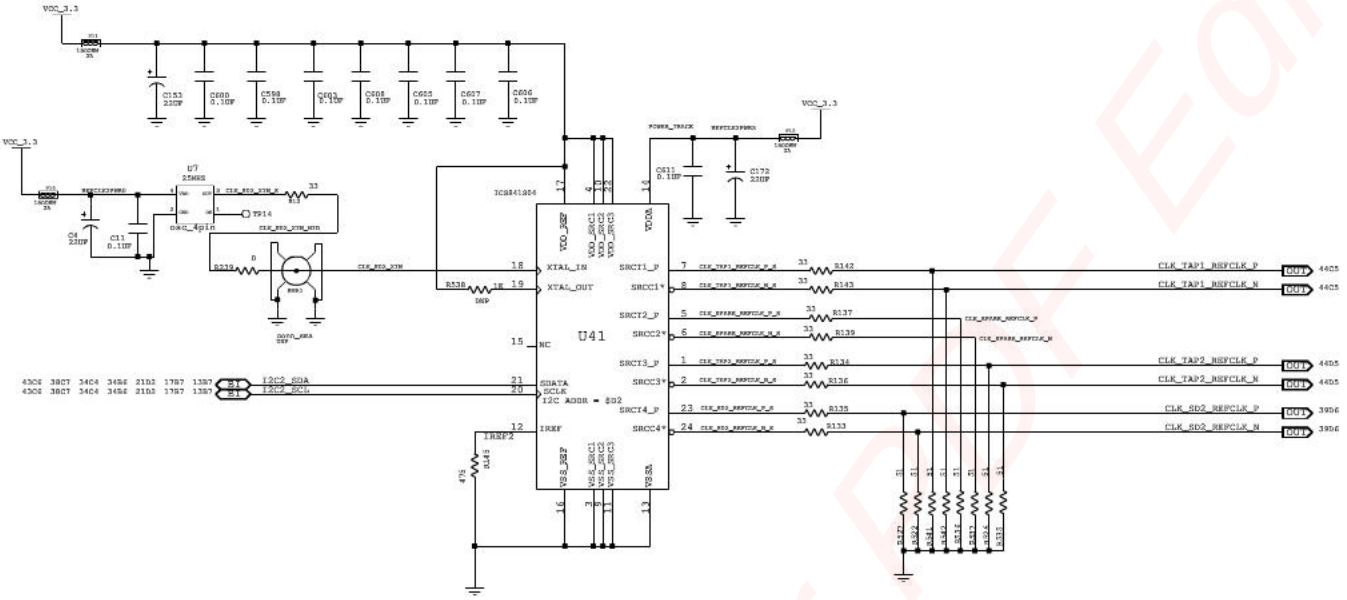
SERDES2 CLOCK



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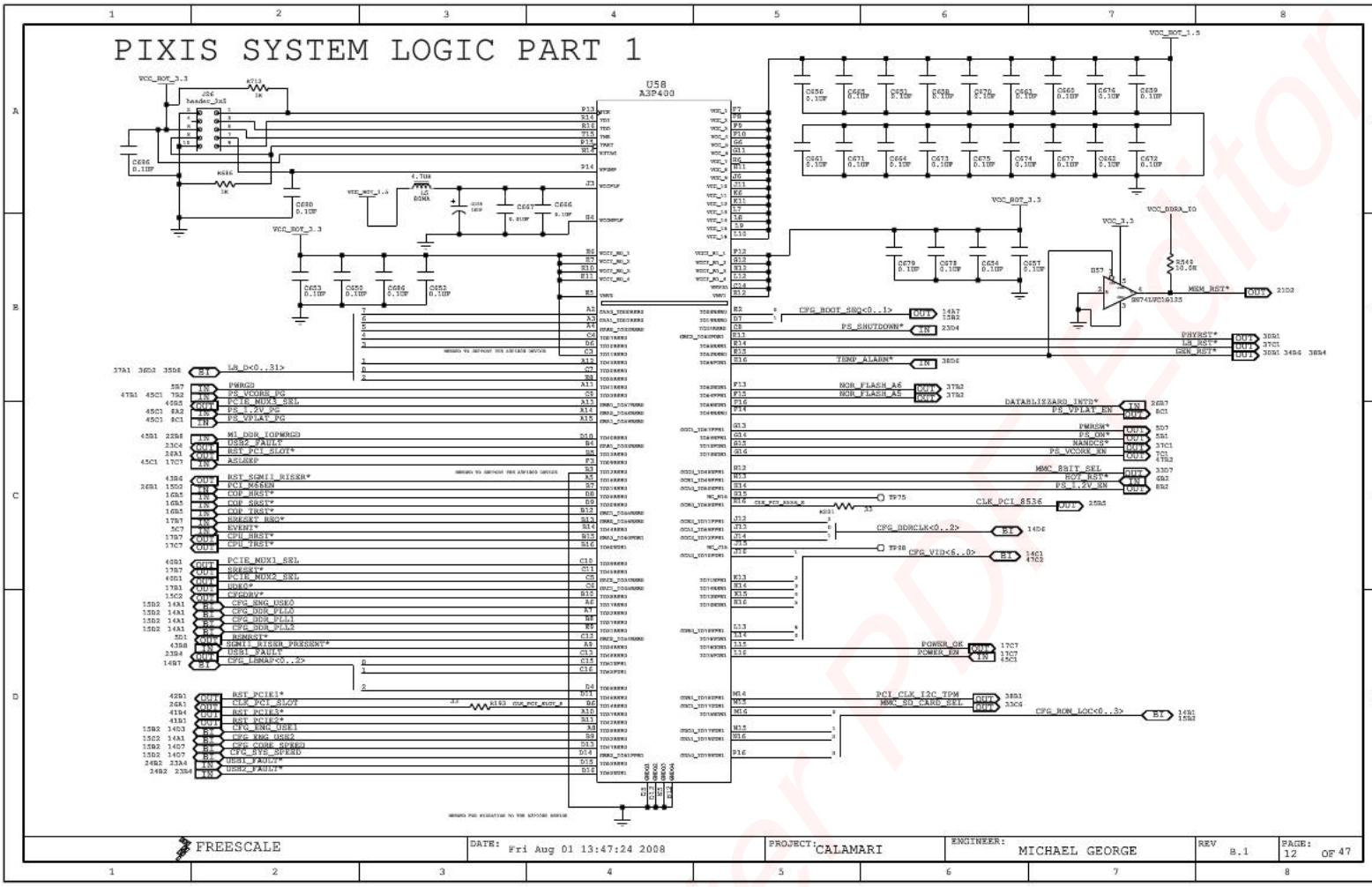
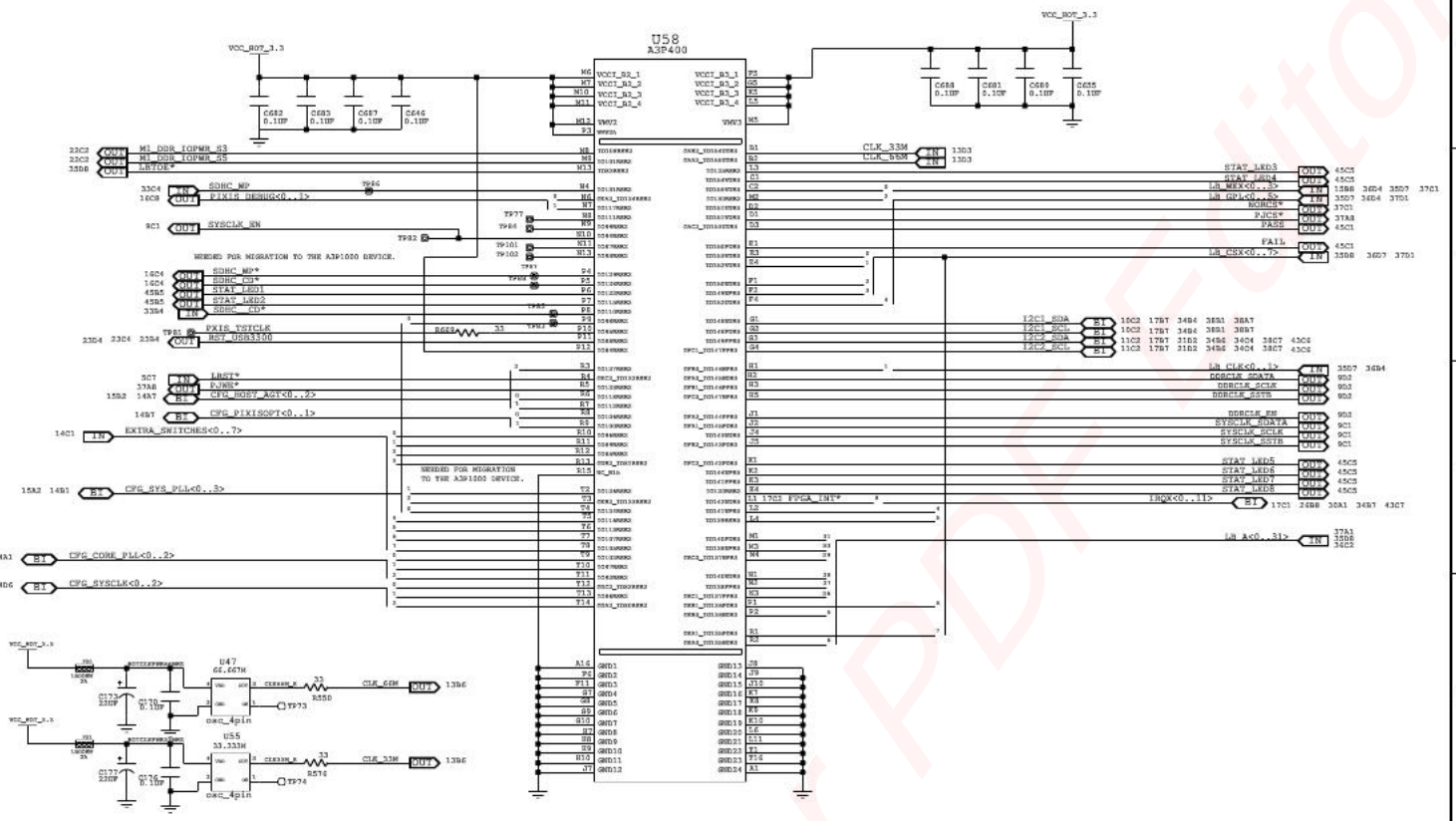


PIXIS SYSTEM LOGIC PART 2



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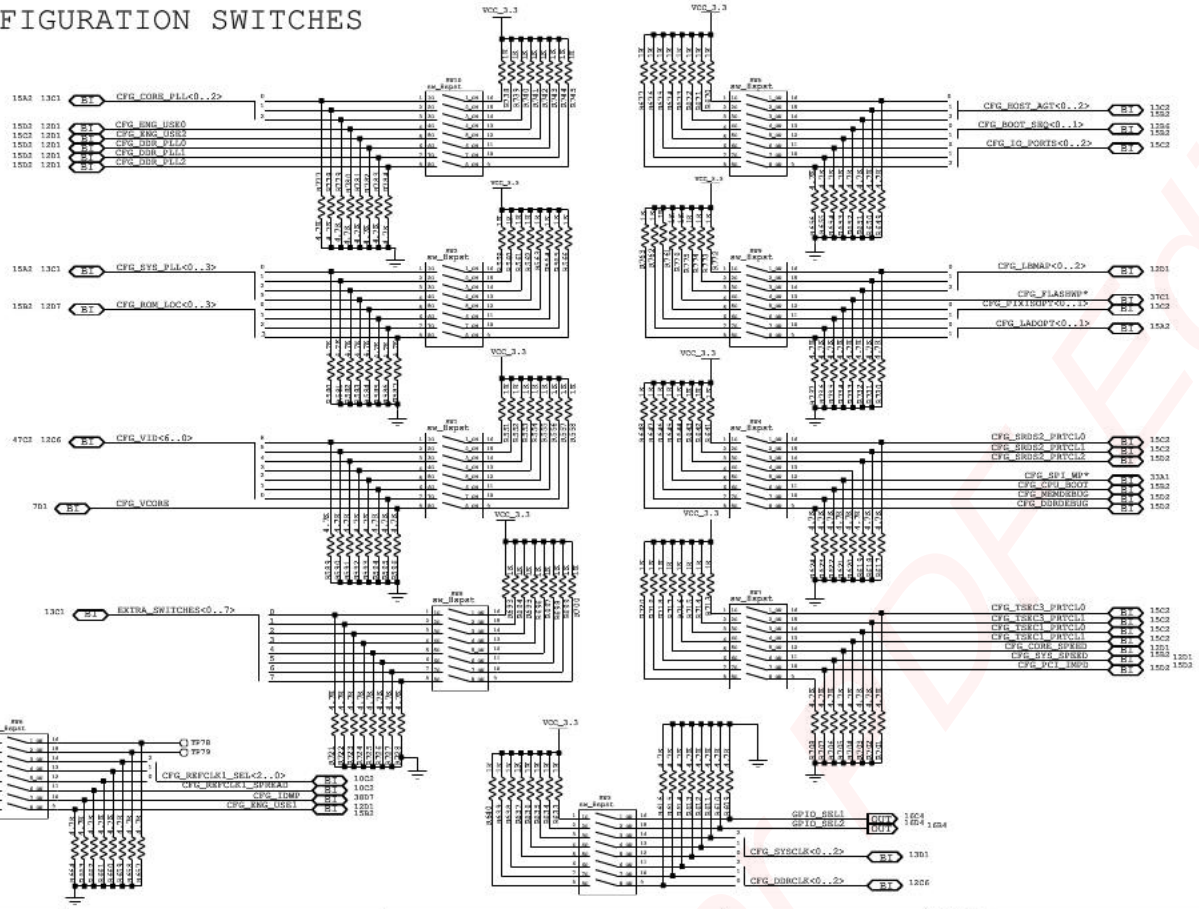
CONFIGURATION SWITCHES



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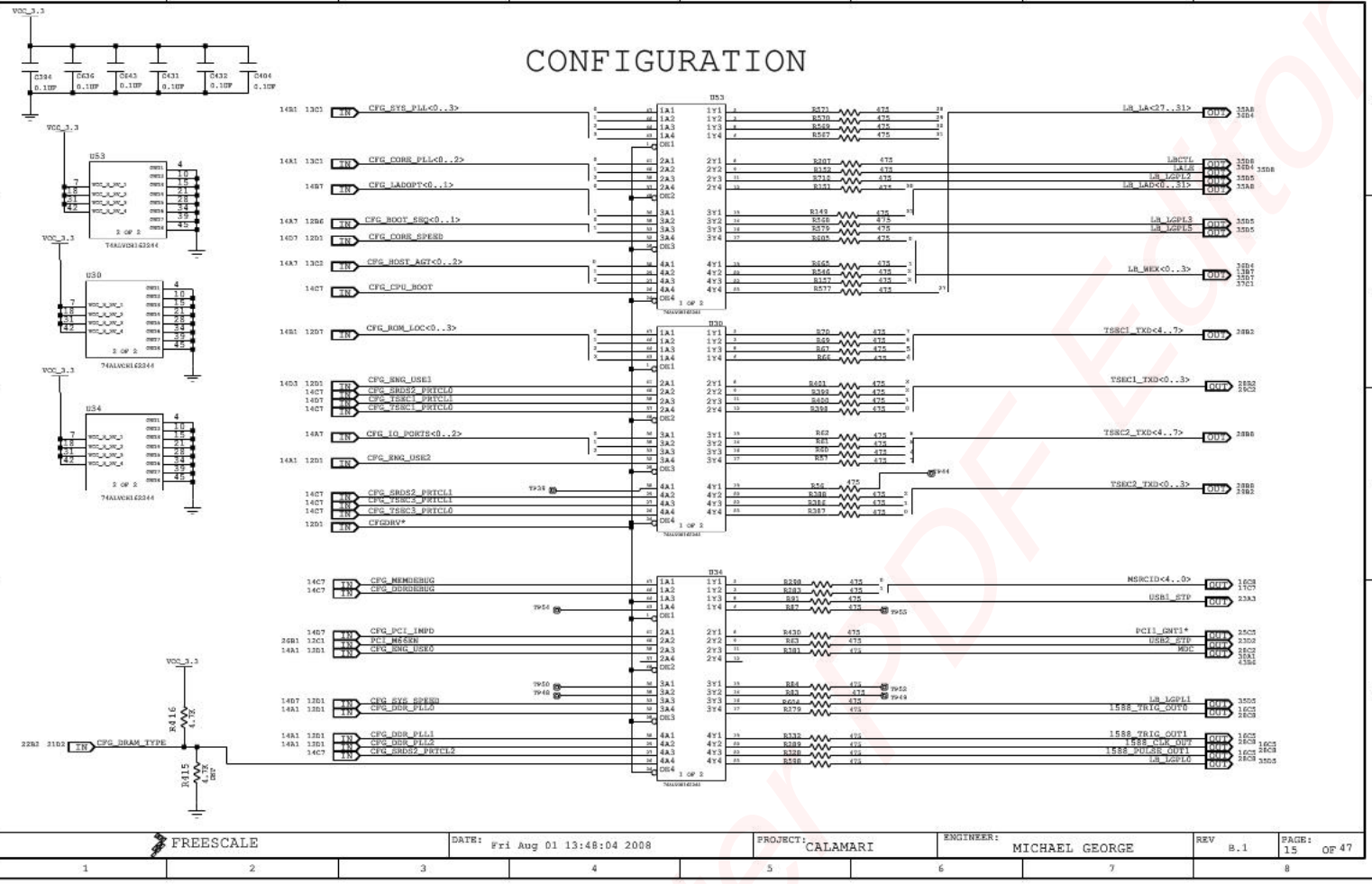
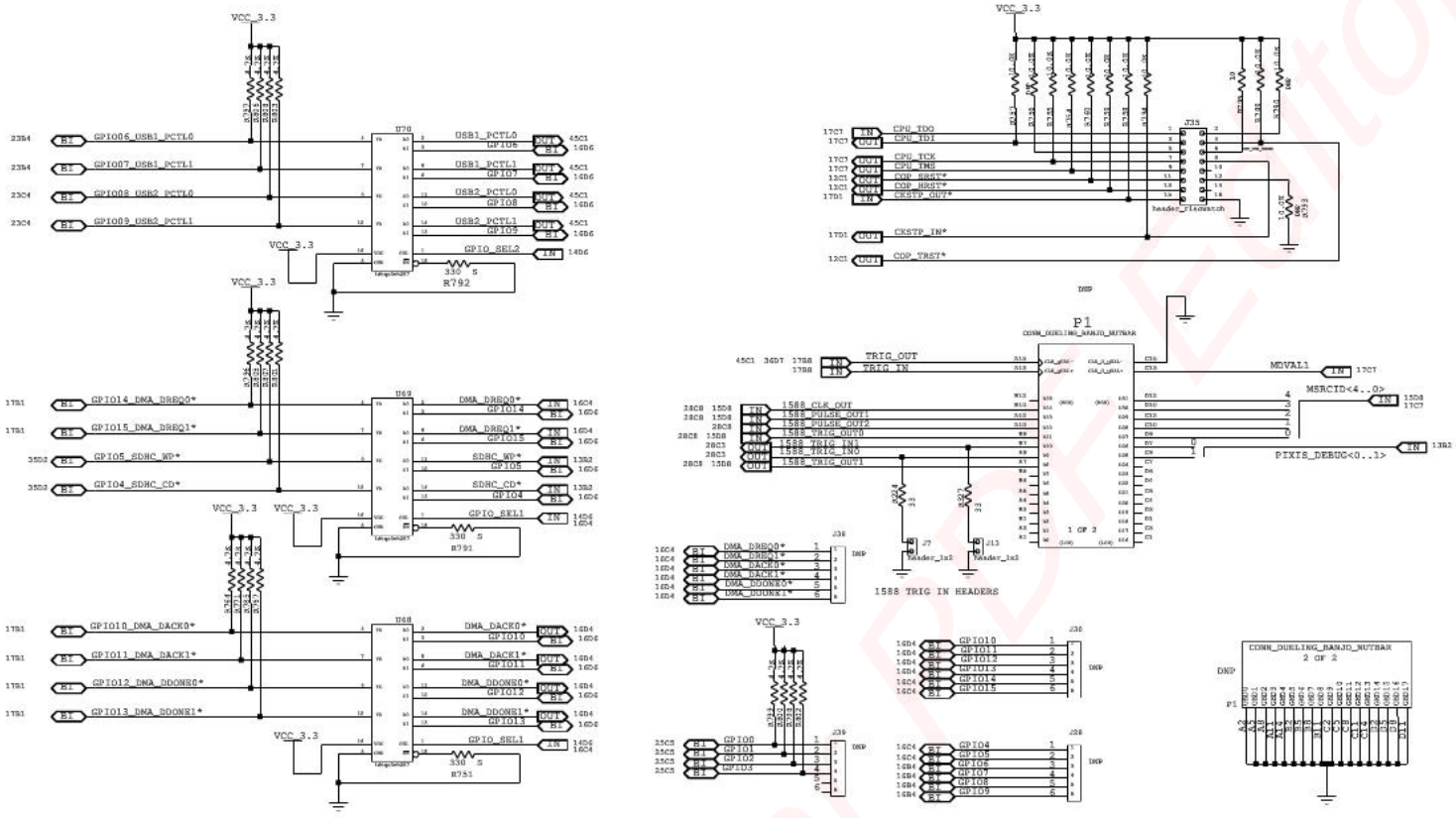
CONFIGURATION



FREESCALE	DATE: Fri Aug 01 13:48:04 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 15 OF 47

JTAG/COP, GPIO, AND 1588 HEADERS



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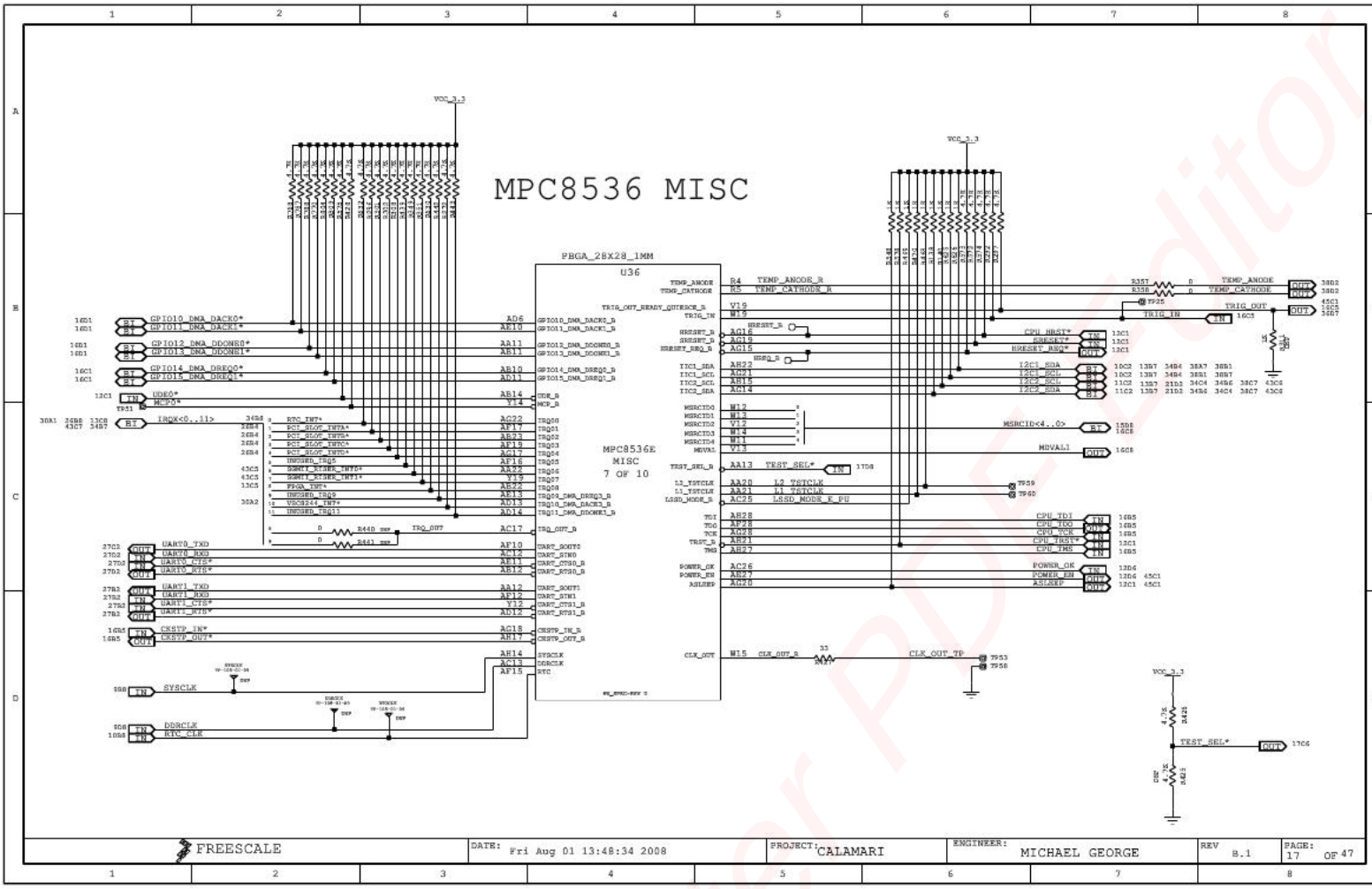

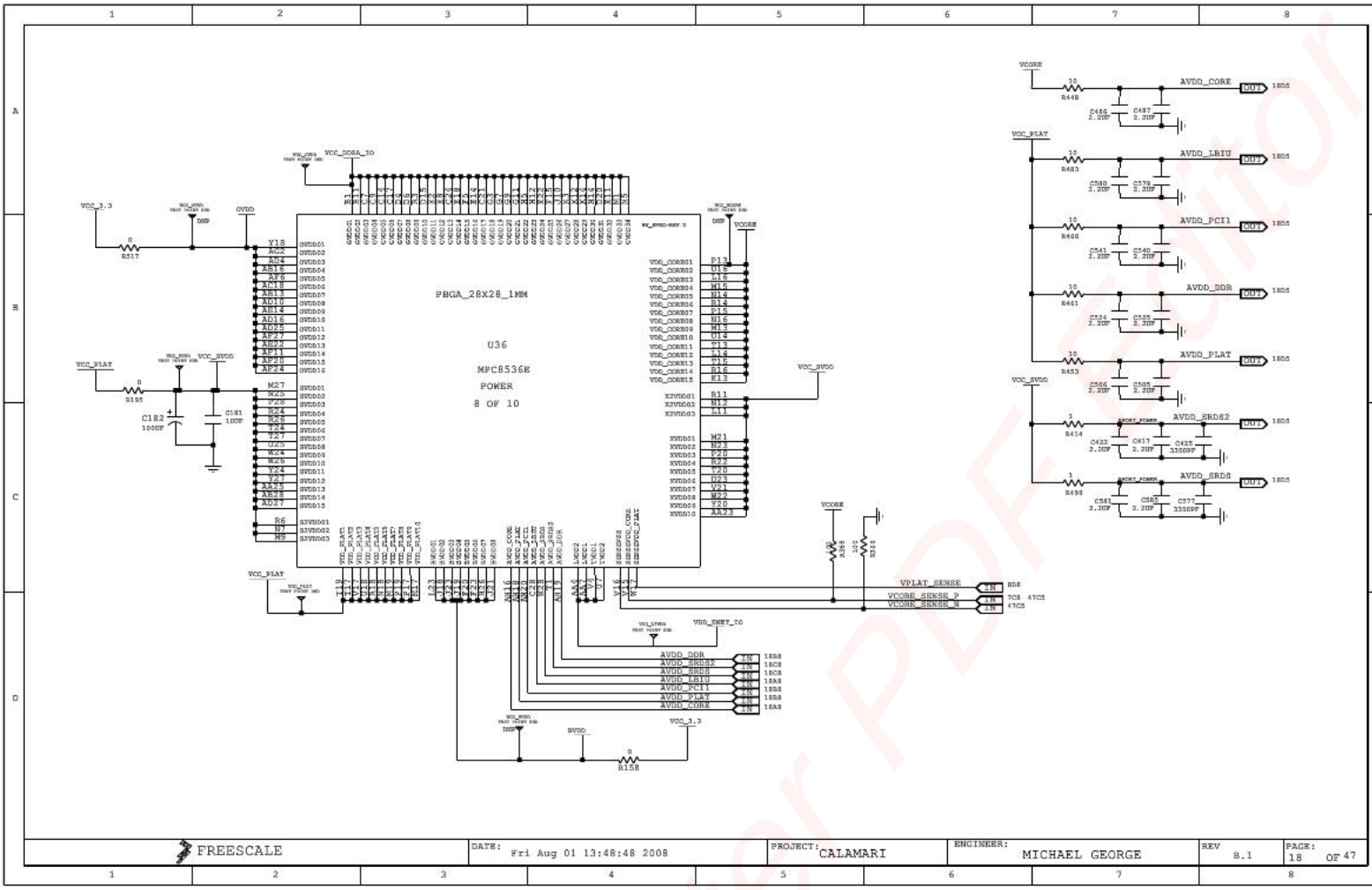

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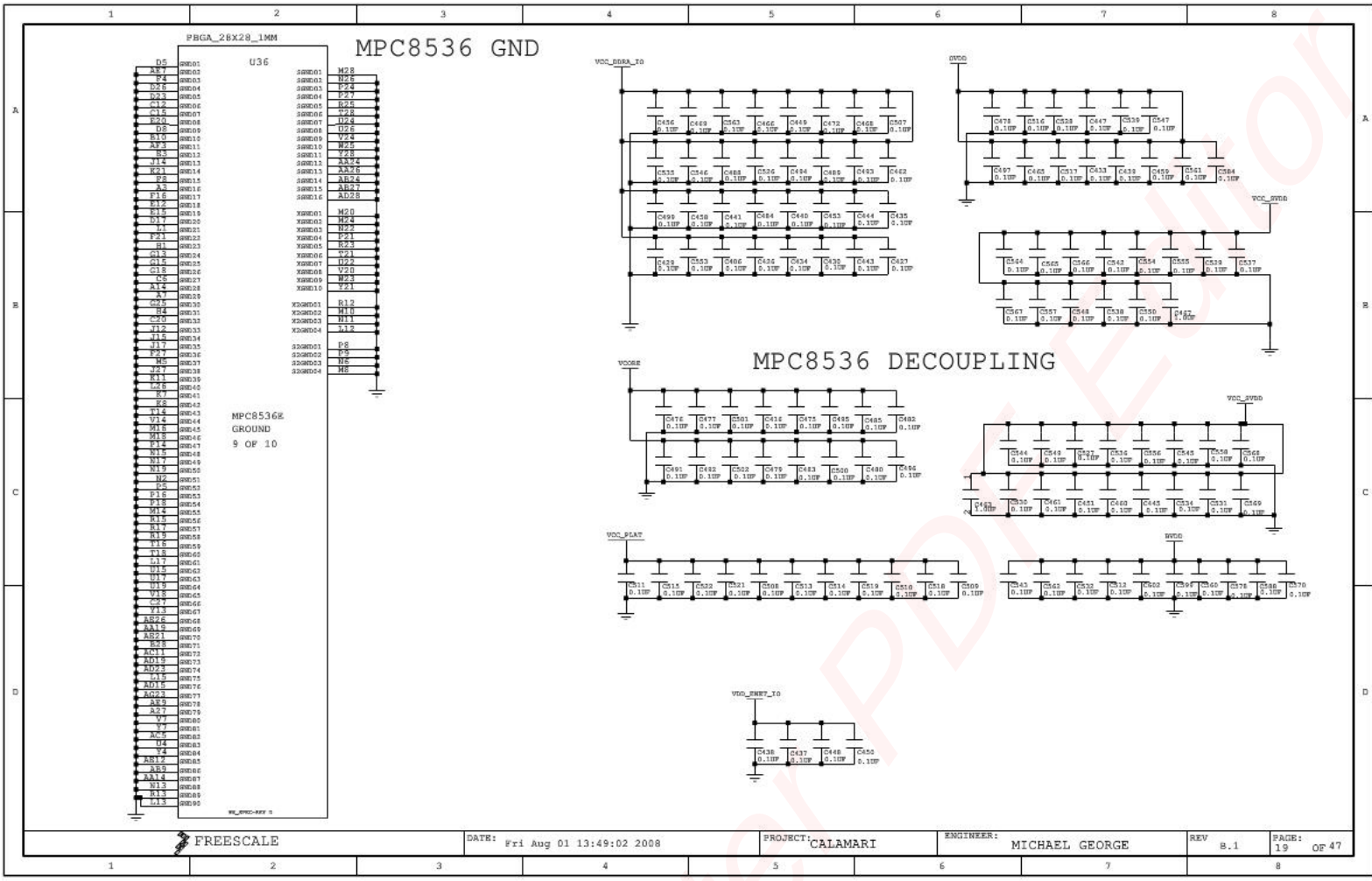

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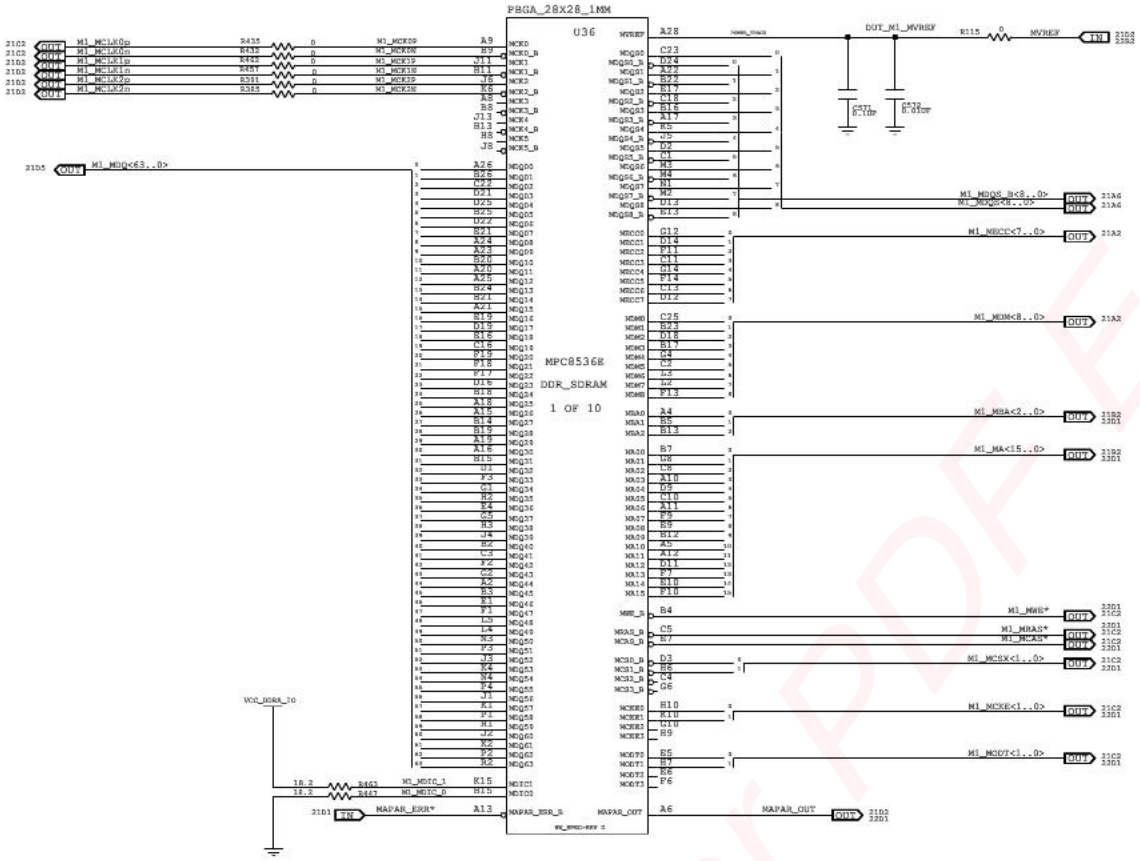
MPC8536 DDR CHANNEL



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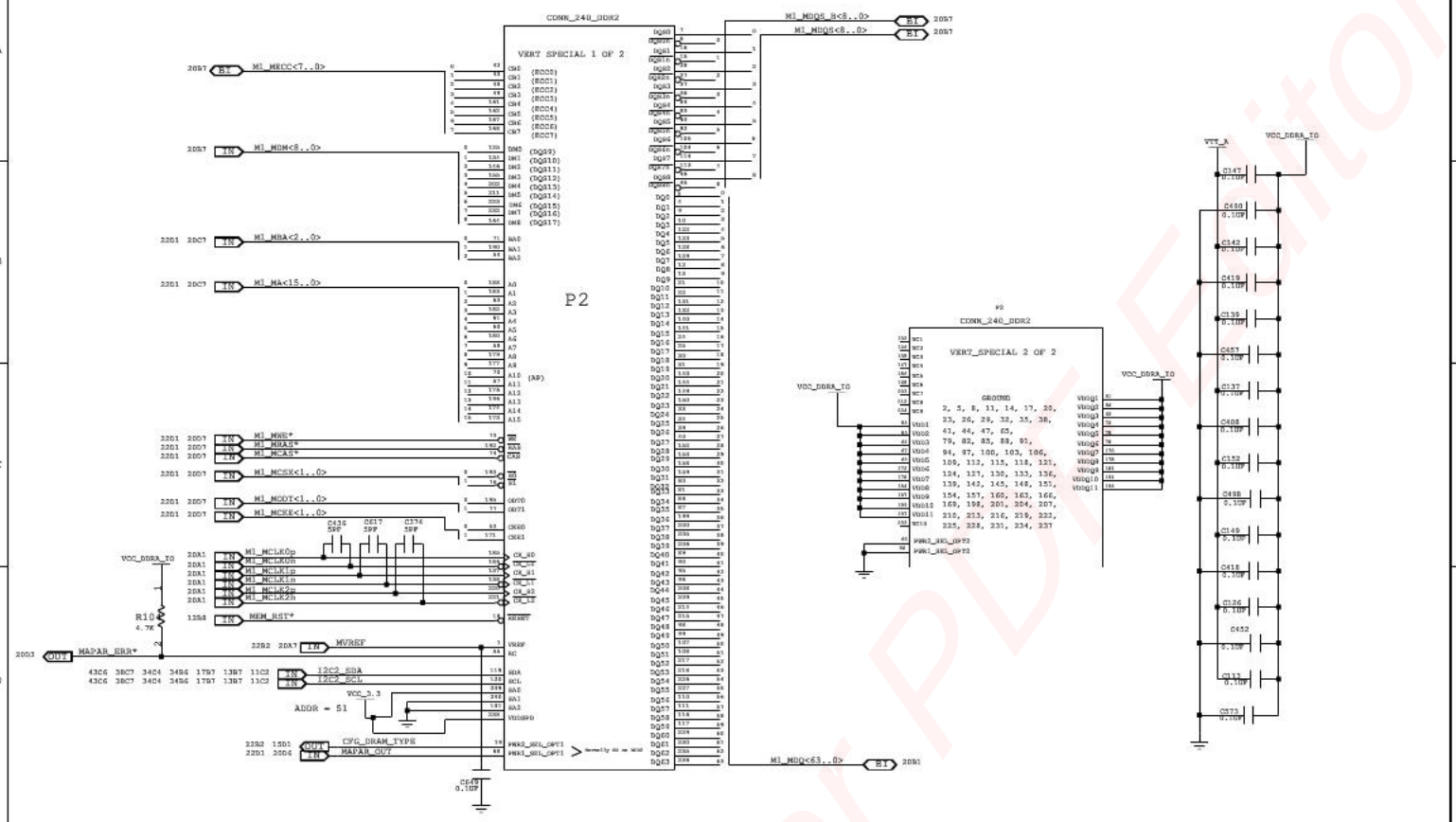
PAGE: 20 OF 47

DDR DIMM



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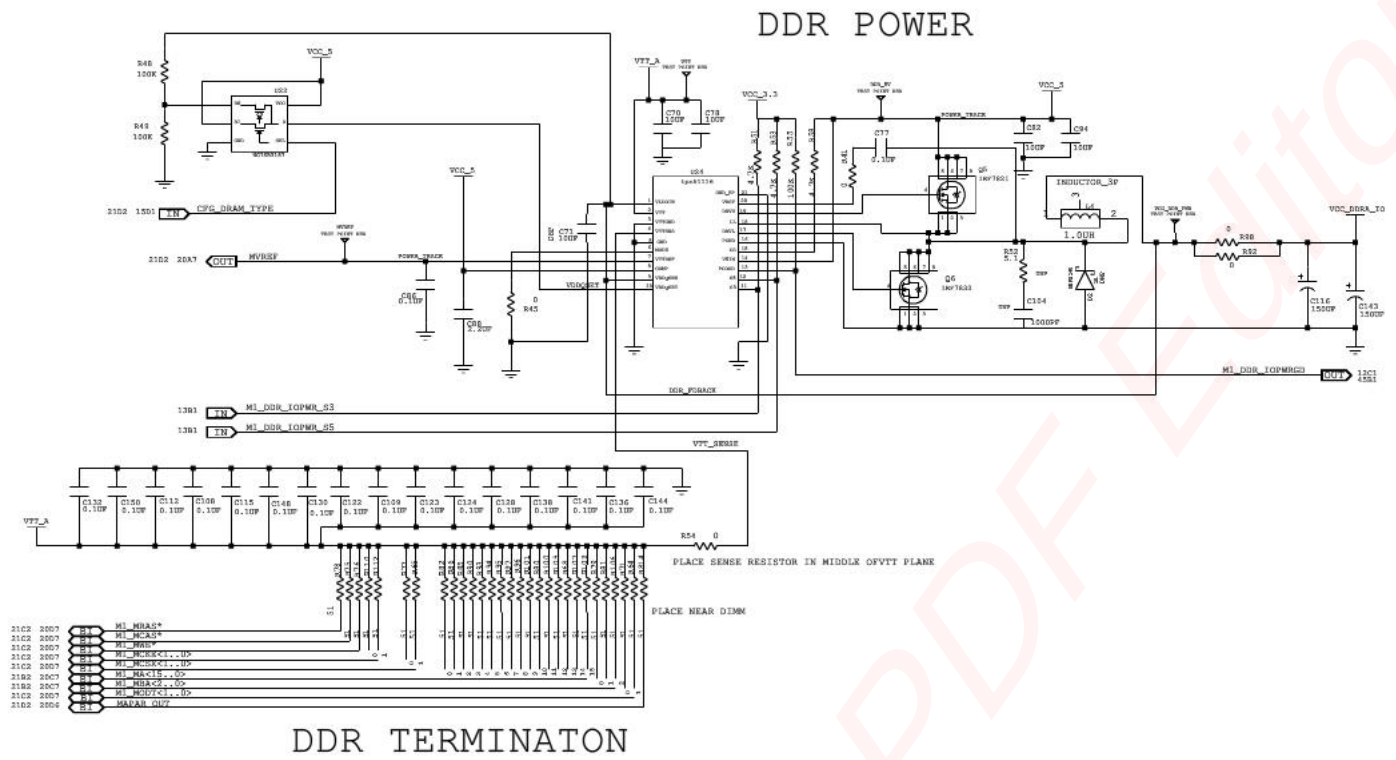

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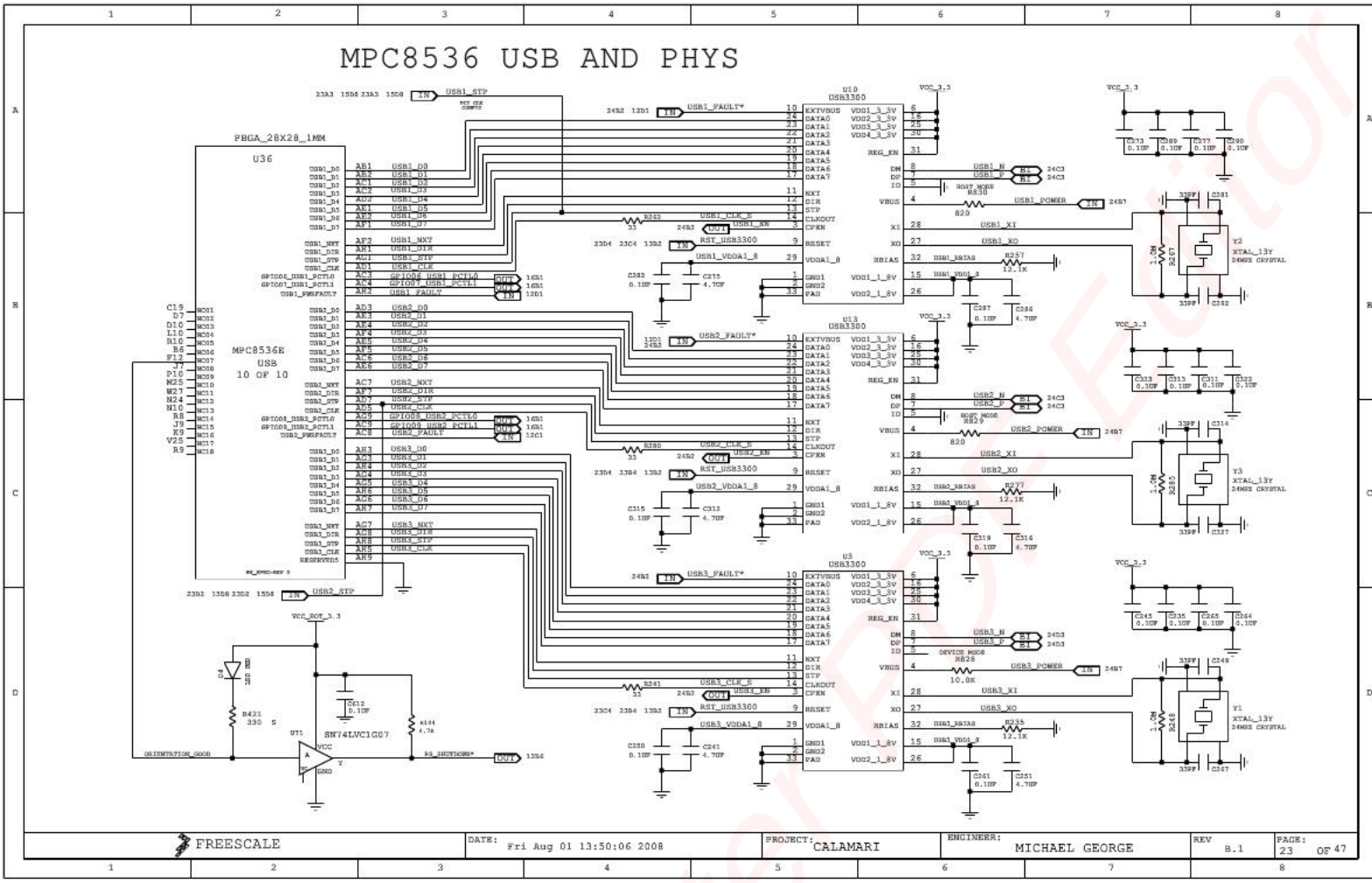
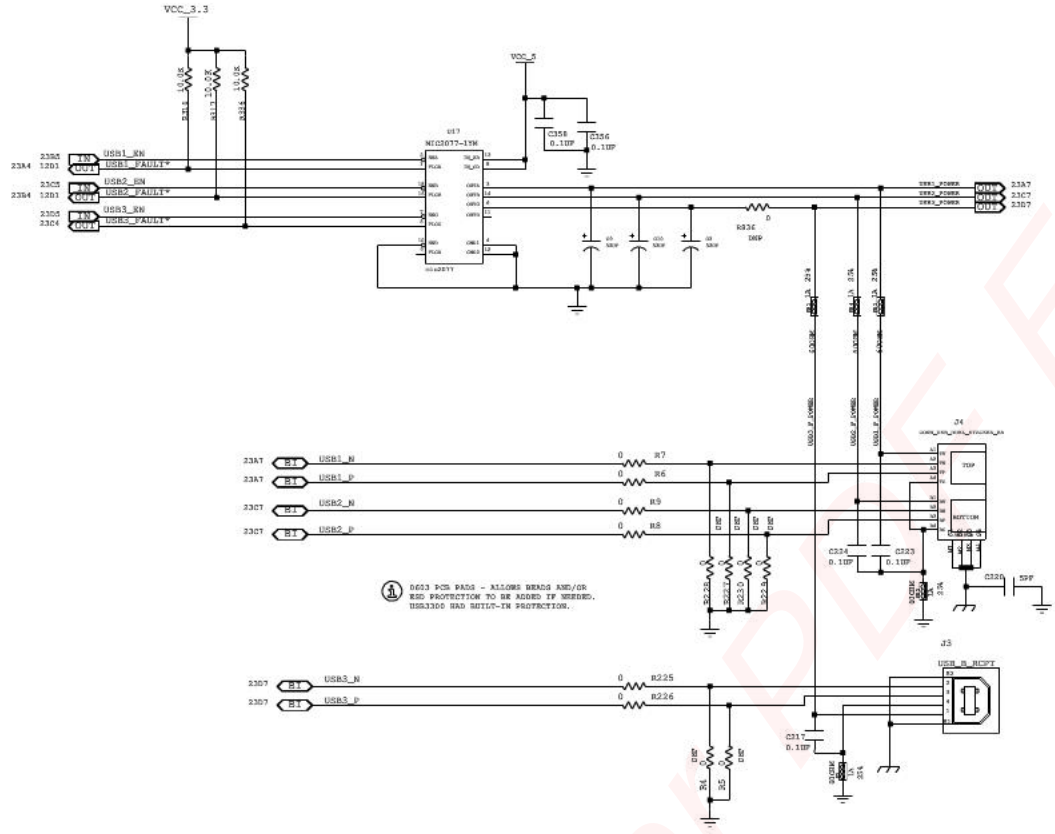


USB PORTS AND POWER



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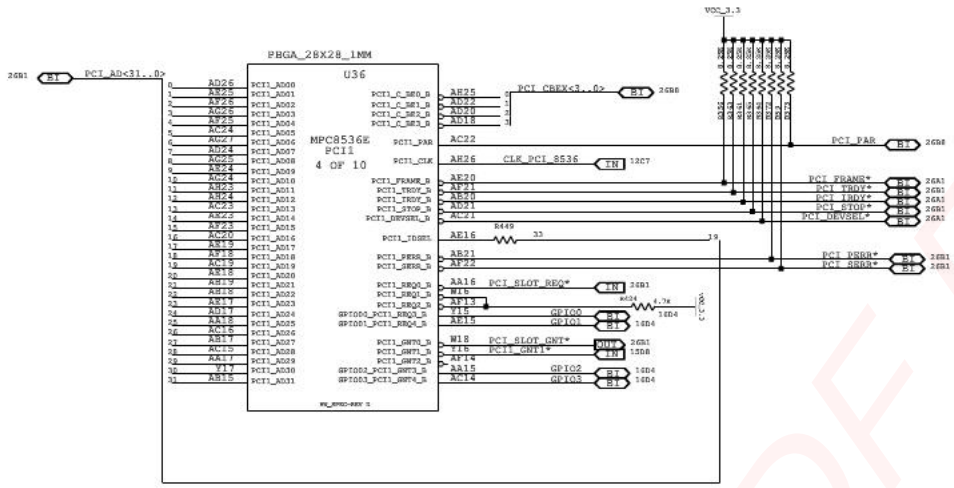
MPC8536 PCI



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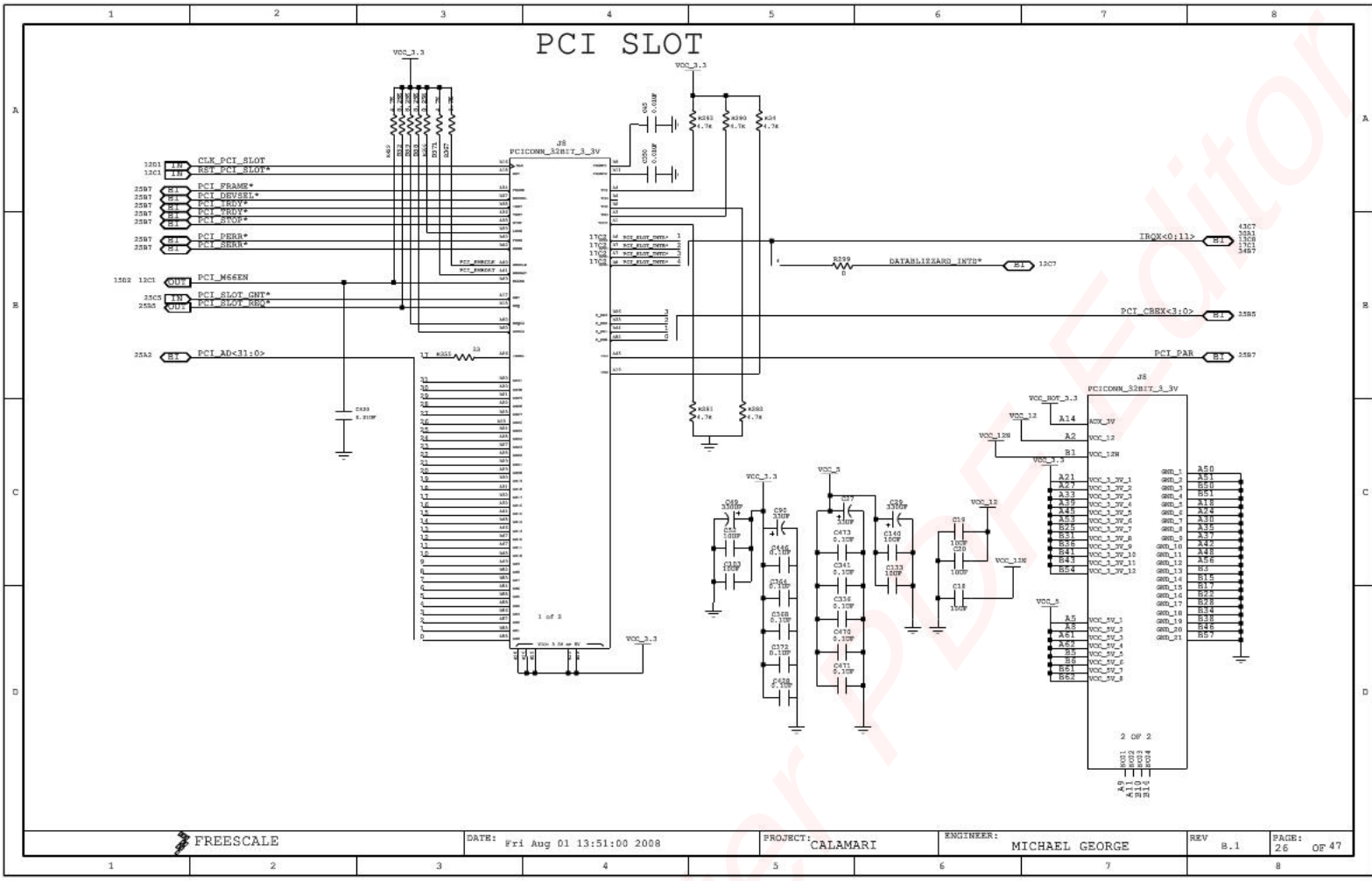
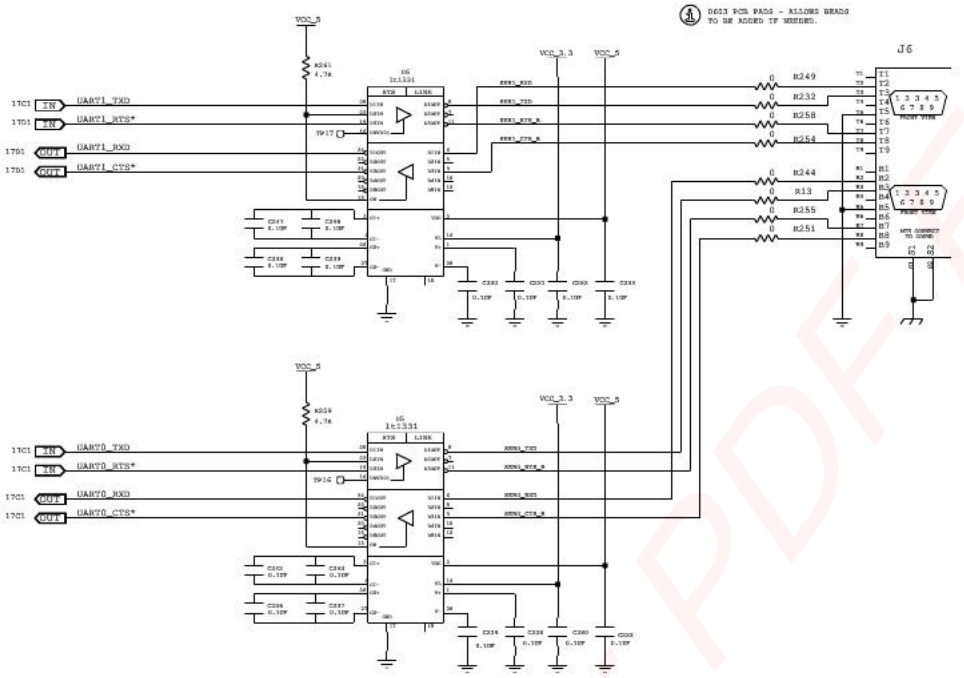
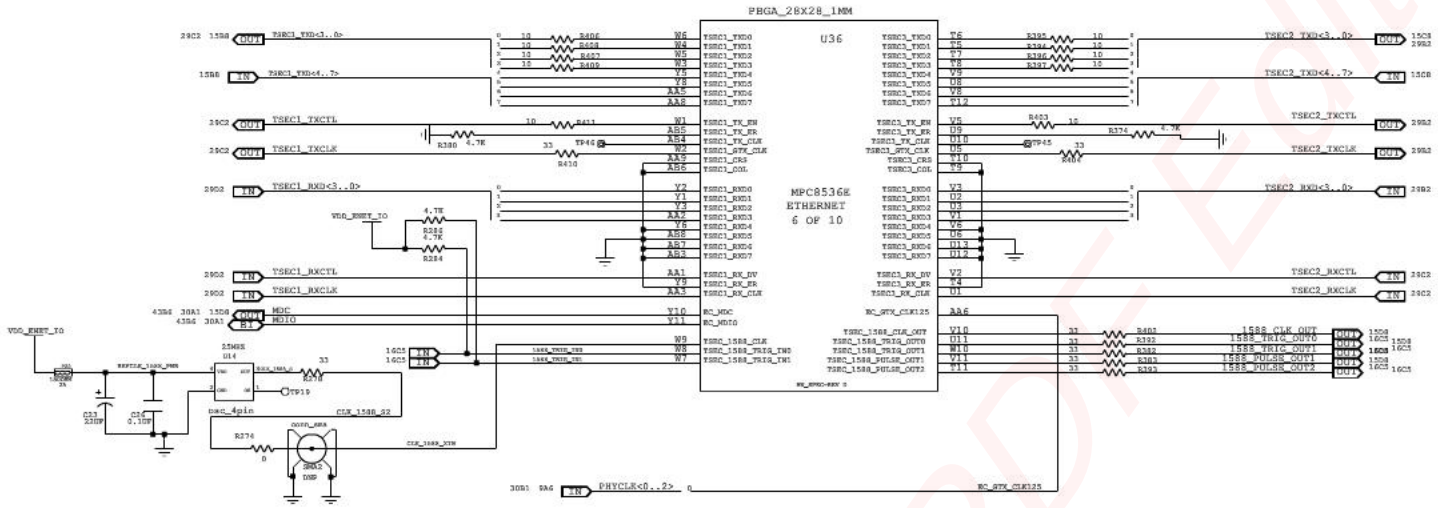


SERIAL PORTS 1 AND 2

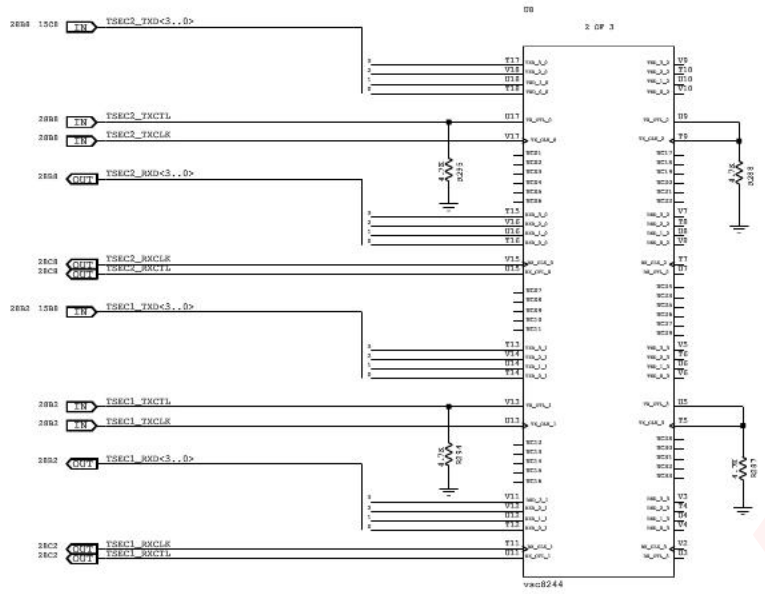


MPC8536 ETHERNET- RGMII



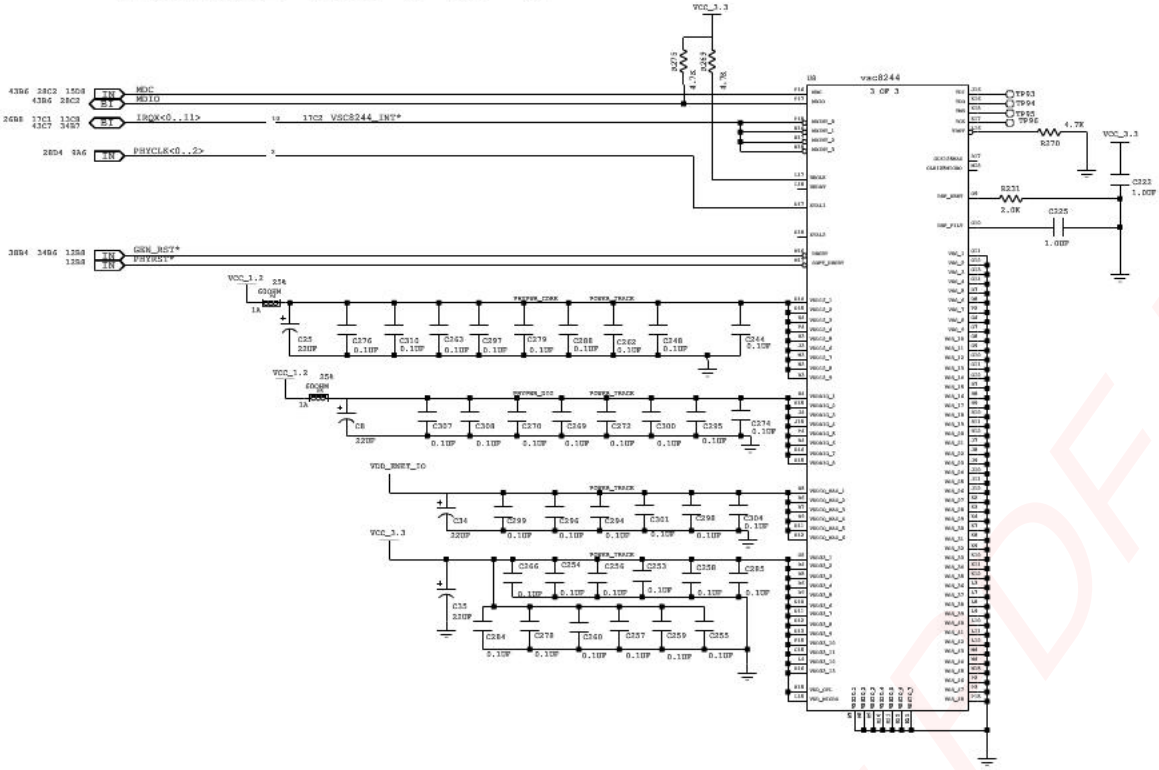
FREESCALE	DATE: Fri Aug 01 13:51:31 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV 8.1	PAGE: 28 OF 47

VITESSE PHY 1 OF 3



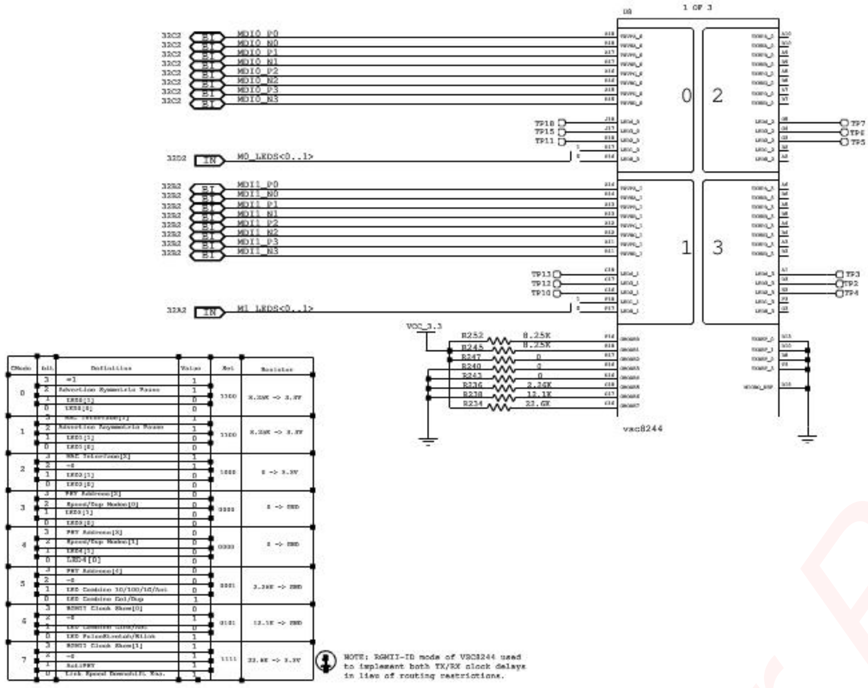
FREESCALE	DATE: Fri Aug 01 13:51:45 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 29 OF 47

VITESSE PHY 2 OF 3



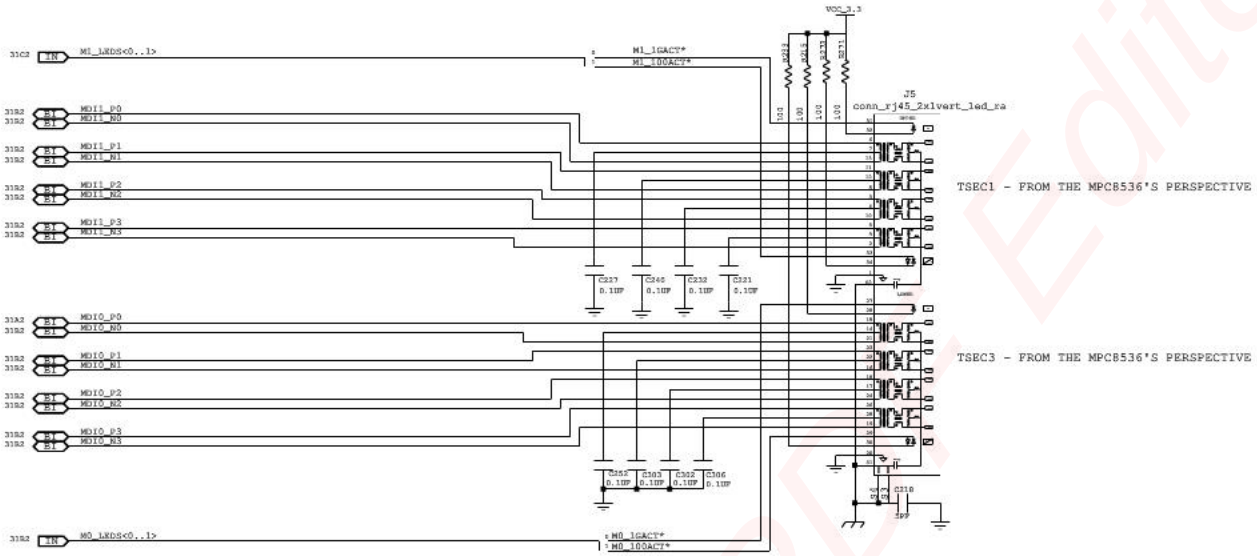
FREESCALE	DATE: Fri Aug 01 13:52:01 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 30 OF 47

VITESSE PHY 3 OF 3

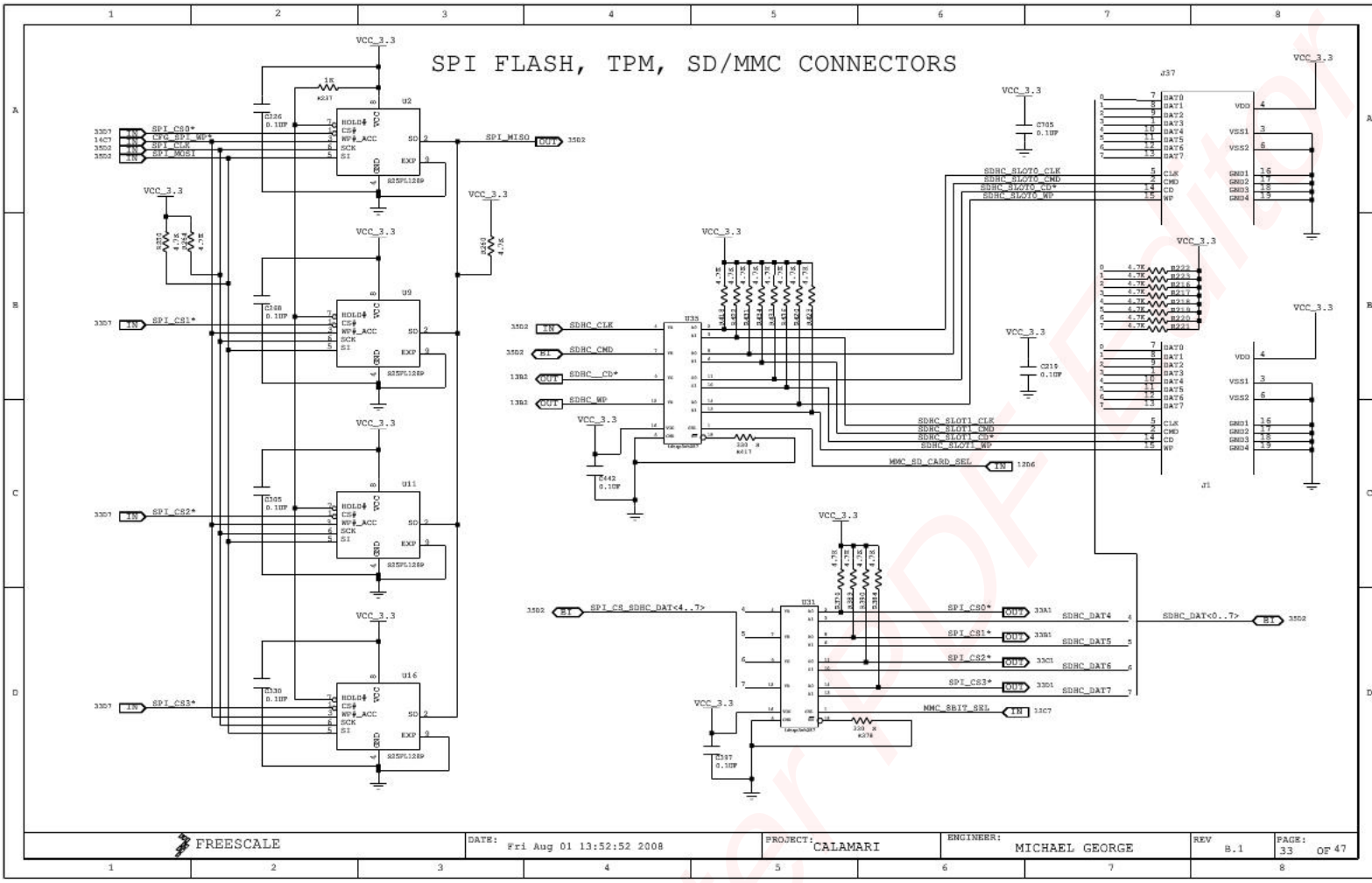


FREESCALE	DATE: Fri Aug 01 13:52:17 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 31 OF 47

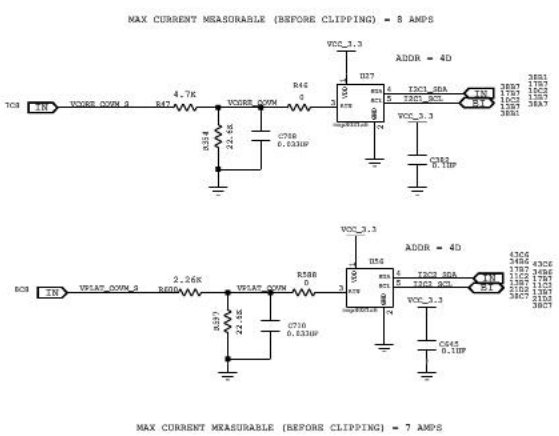
ETHERNET PORT CONNECTORS

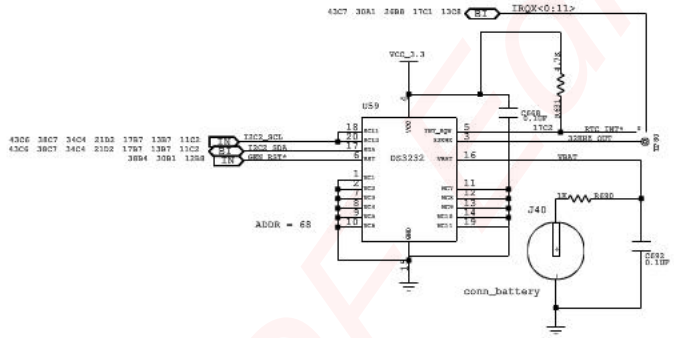


FREESCALE	DATE: Fri Aug 01 13:52:33 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 32 OF 47



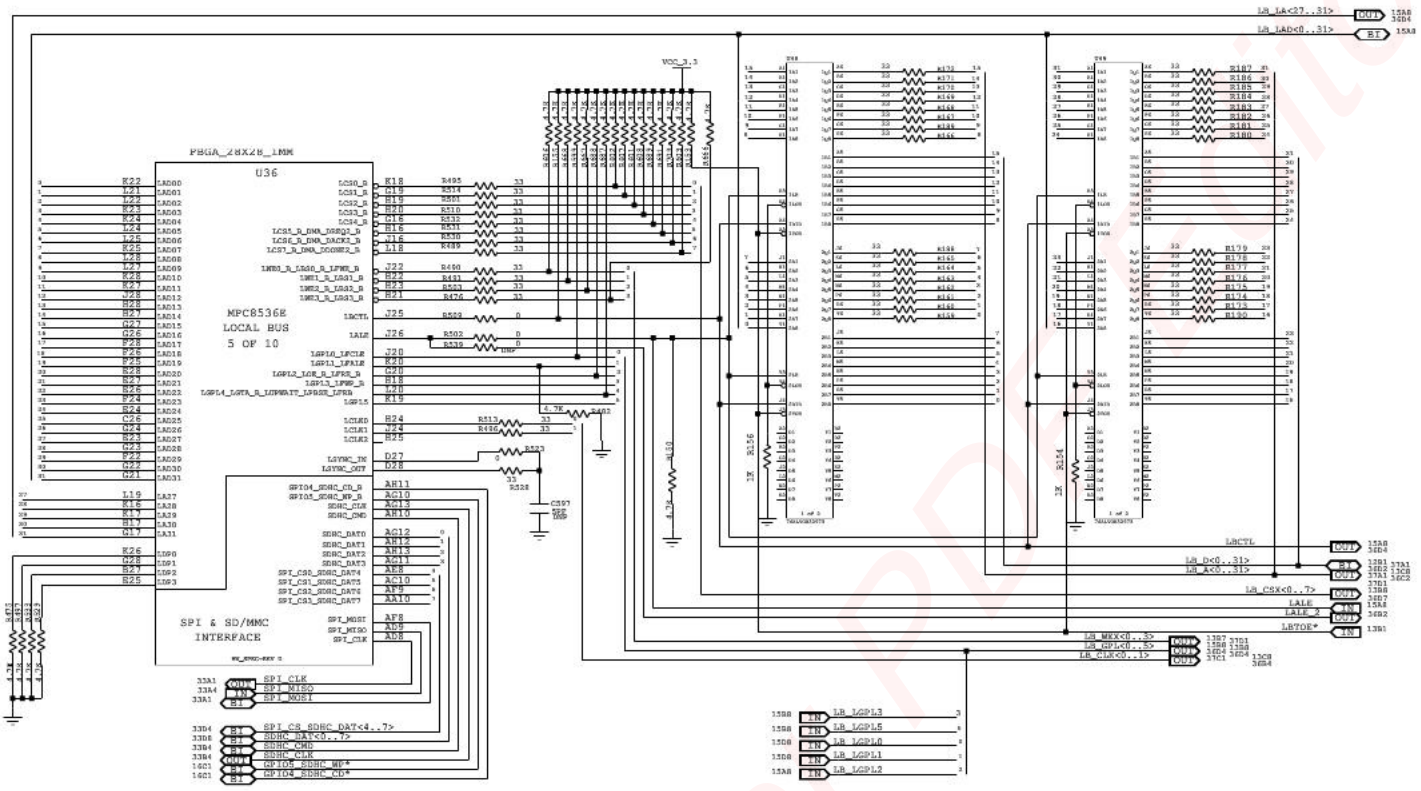
RTC/NVRAM WITH BATTERY, I2C A/D'S





FREESCALE	DATE: Fri Aug 01 13:53:12 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 34 OF 47

MPC8536 LOCAL BUS, SPI, SD INTERFACES



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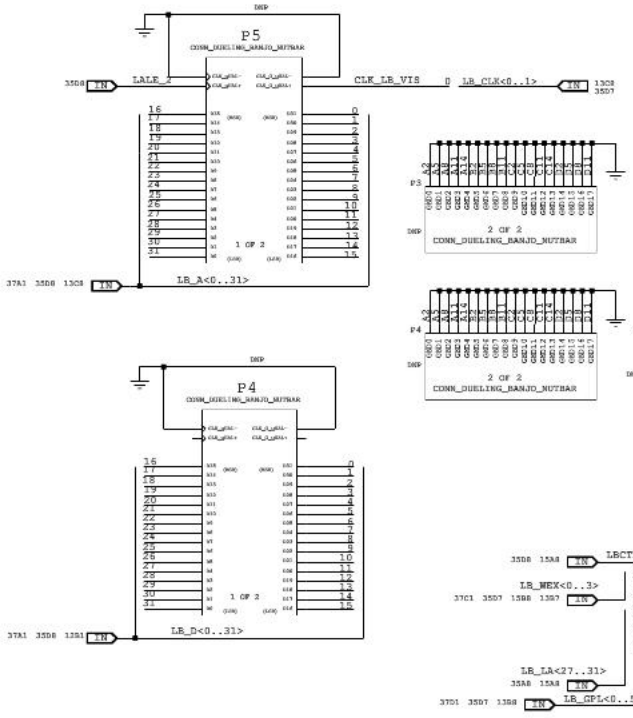
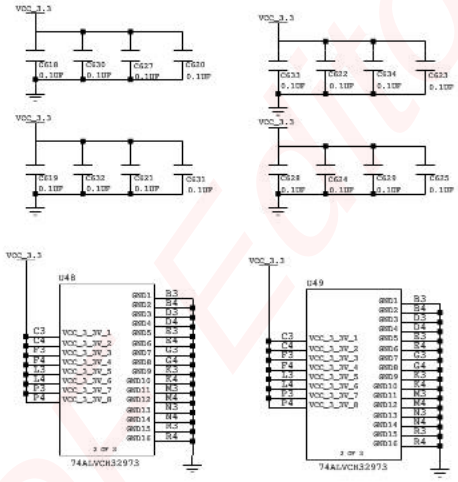
PAGE: 35 OF 47

LB VISIBILITY

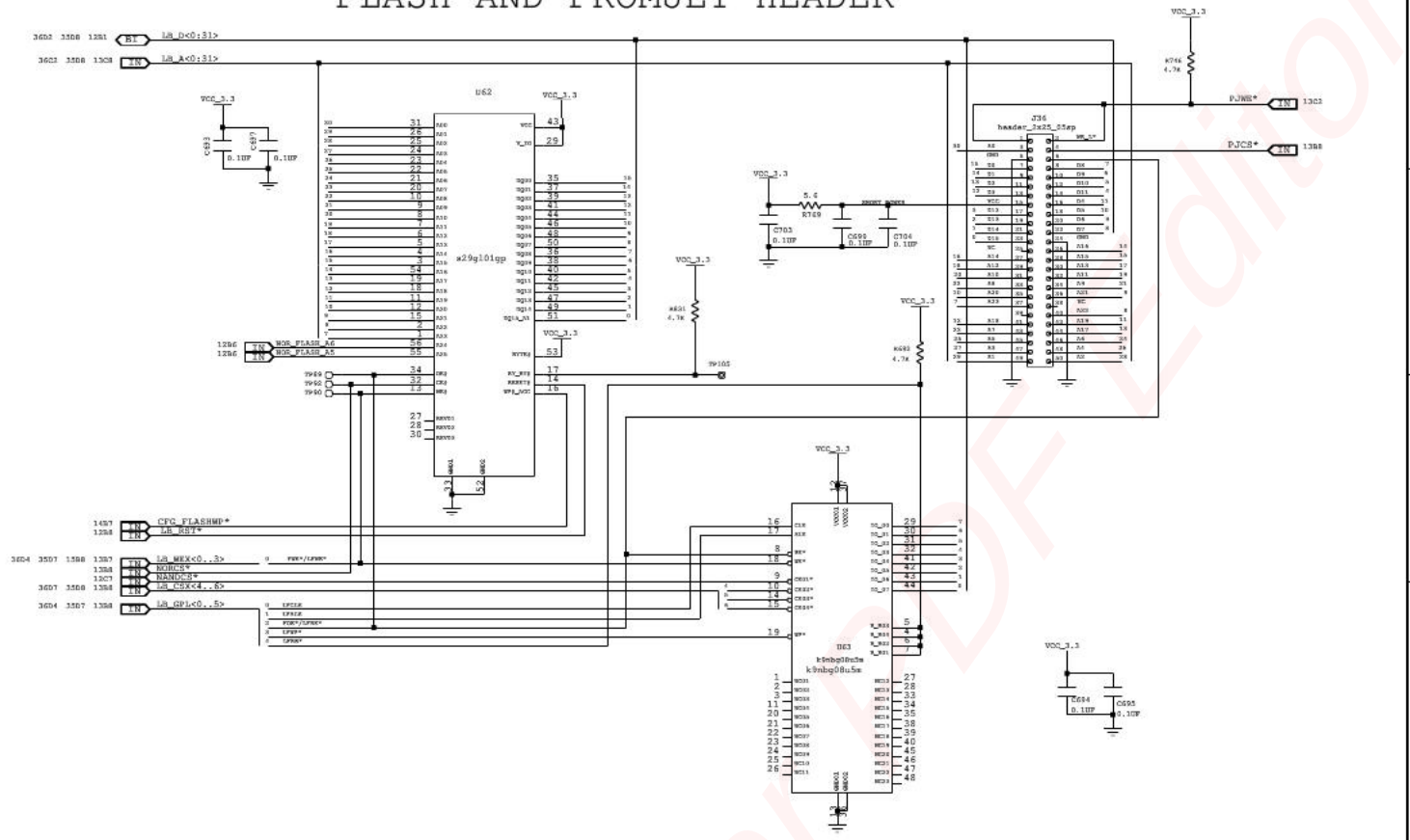


LBC BUFFER POWER



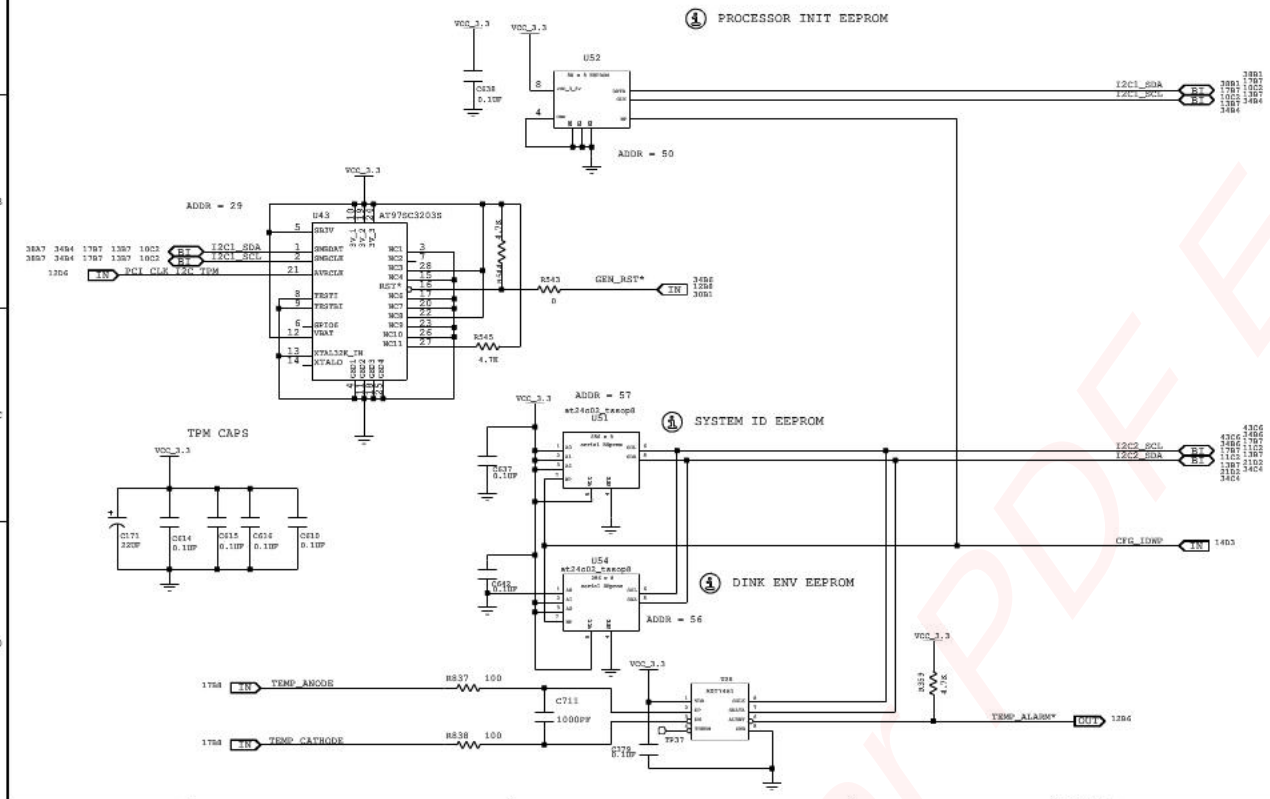
FREESCALE	DATE: Fri Aug 01 13:53:47 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 36 OF 47

FLASH AND PROMJET HEADER



FREESCALE	DATE: Thu Aug 07 10:06:14 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 37 OF 47

I2C DEVICES



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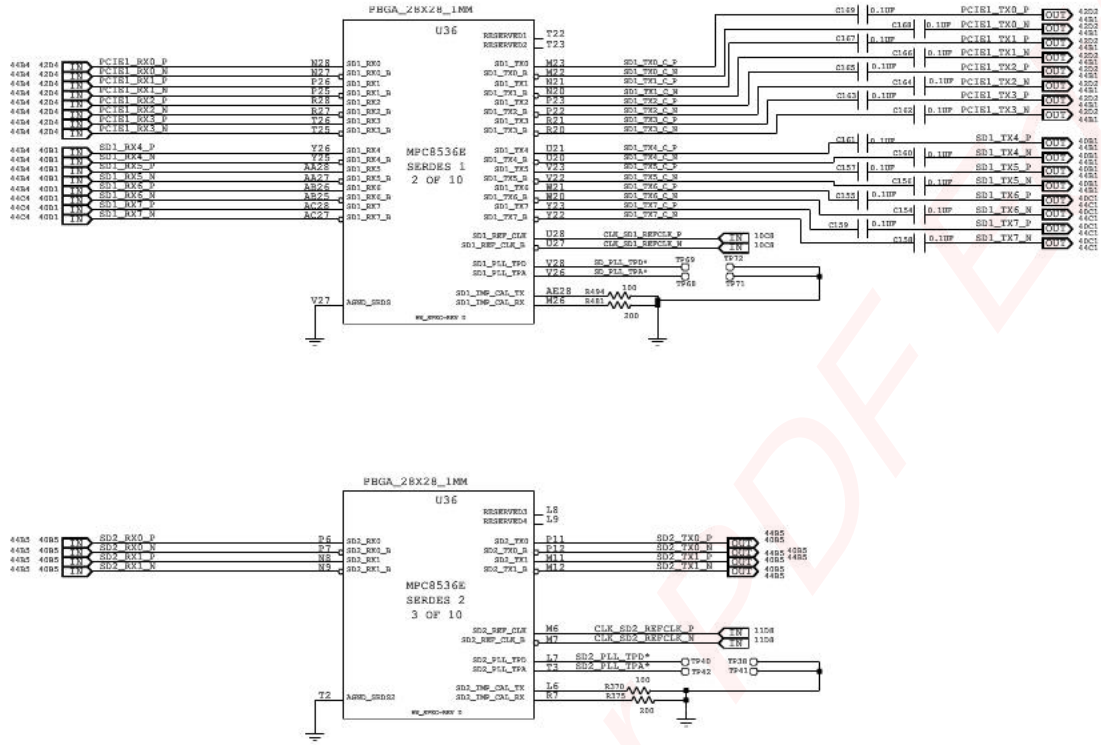
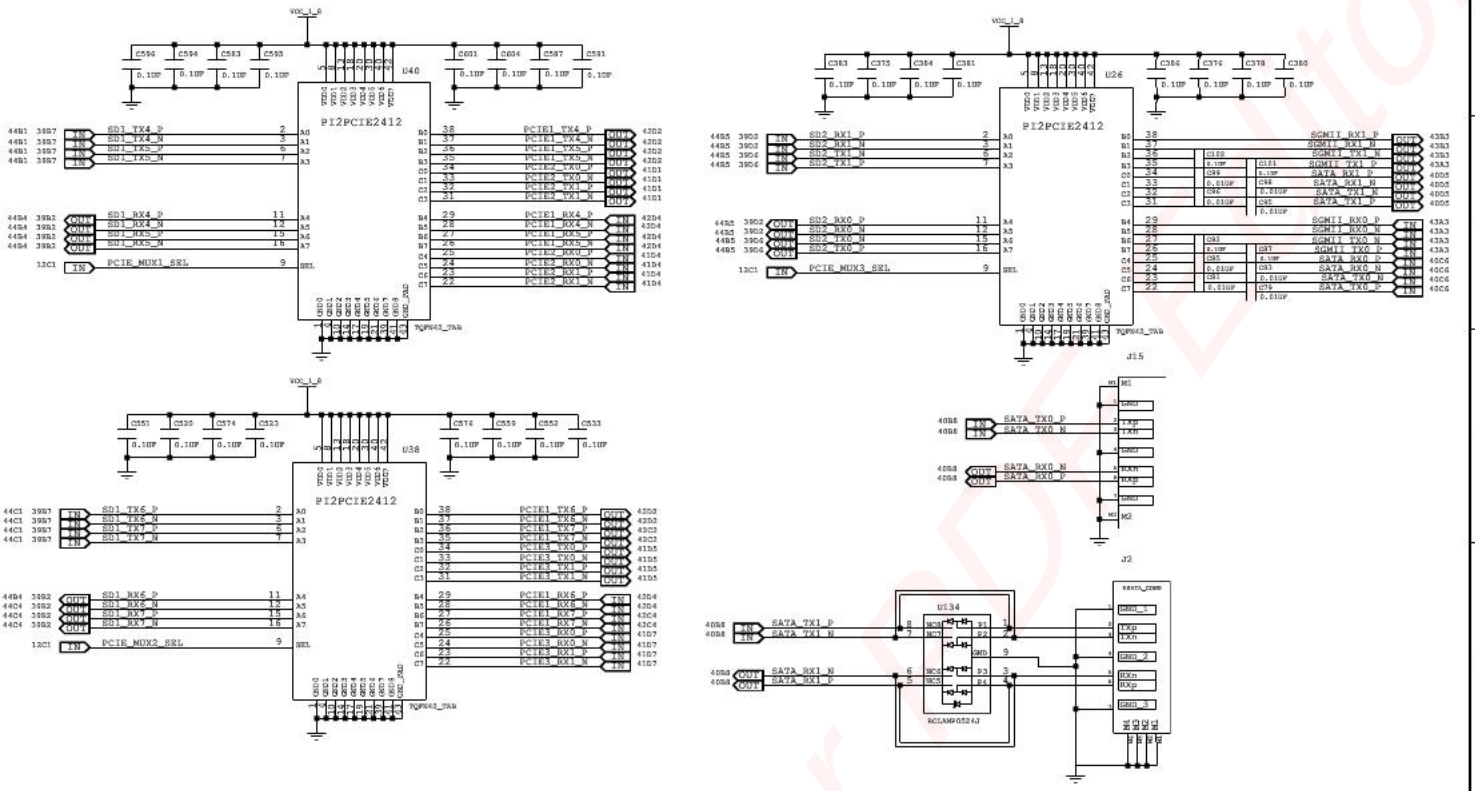
MPC8536 SERDES



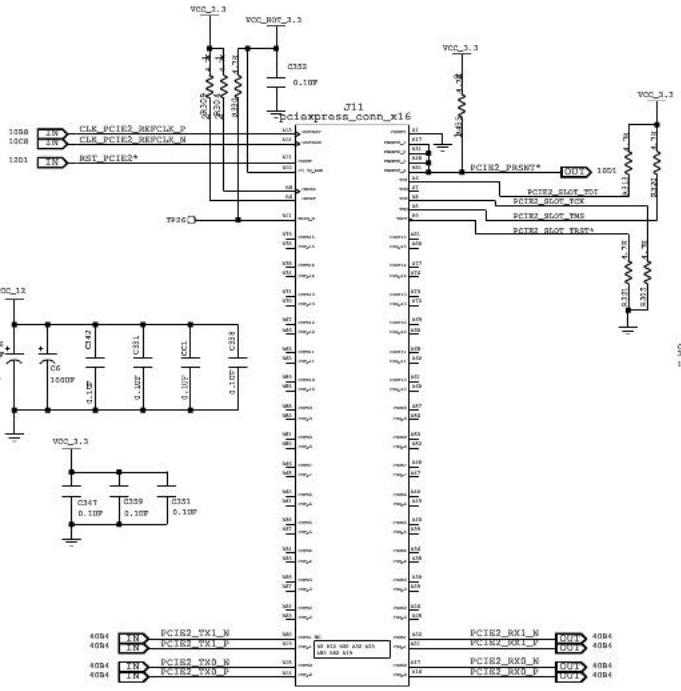
FREESCALE	DATE: Fri Aug 01 13:54:45 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV 8.1	PAGE: 39 OF 47

HIGH SPEED MUXES AND SATA CONNECTORS

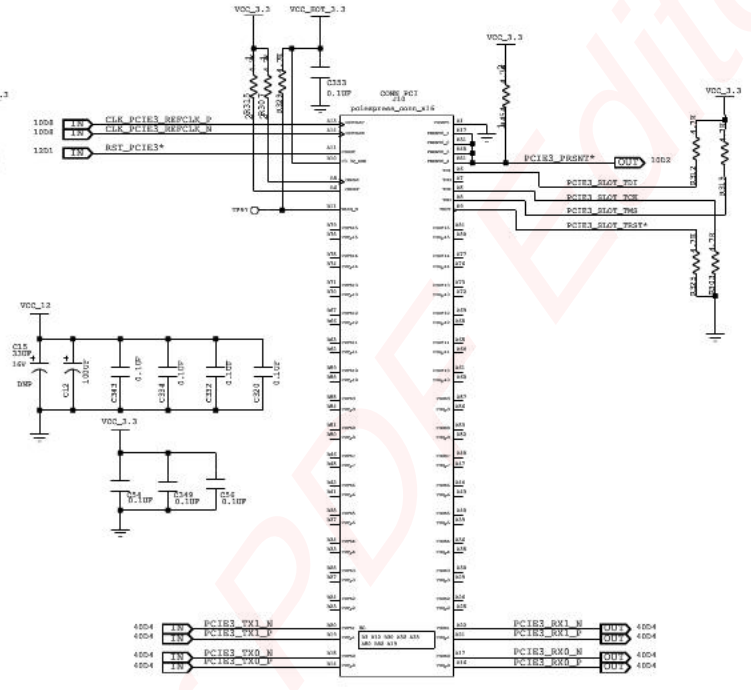


FREESCALE	DATE: Fri Aug 01 13:43:09 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 40 OF 47

PCIEXPRESS SLOTS

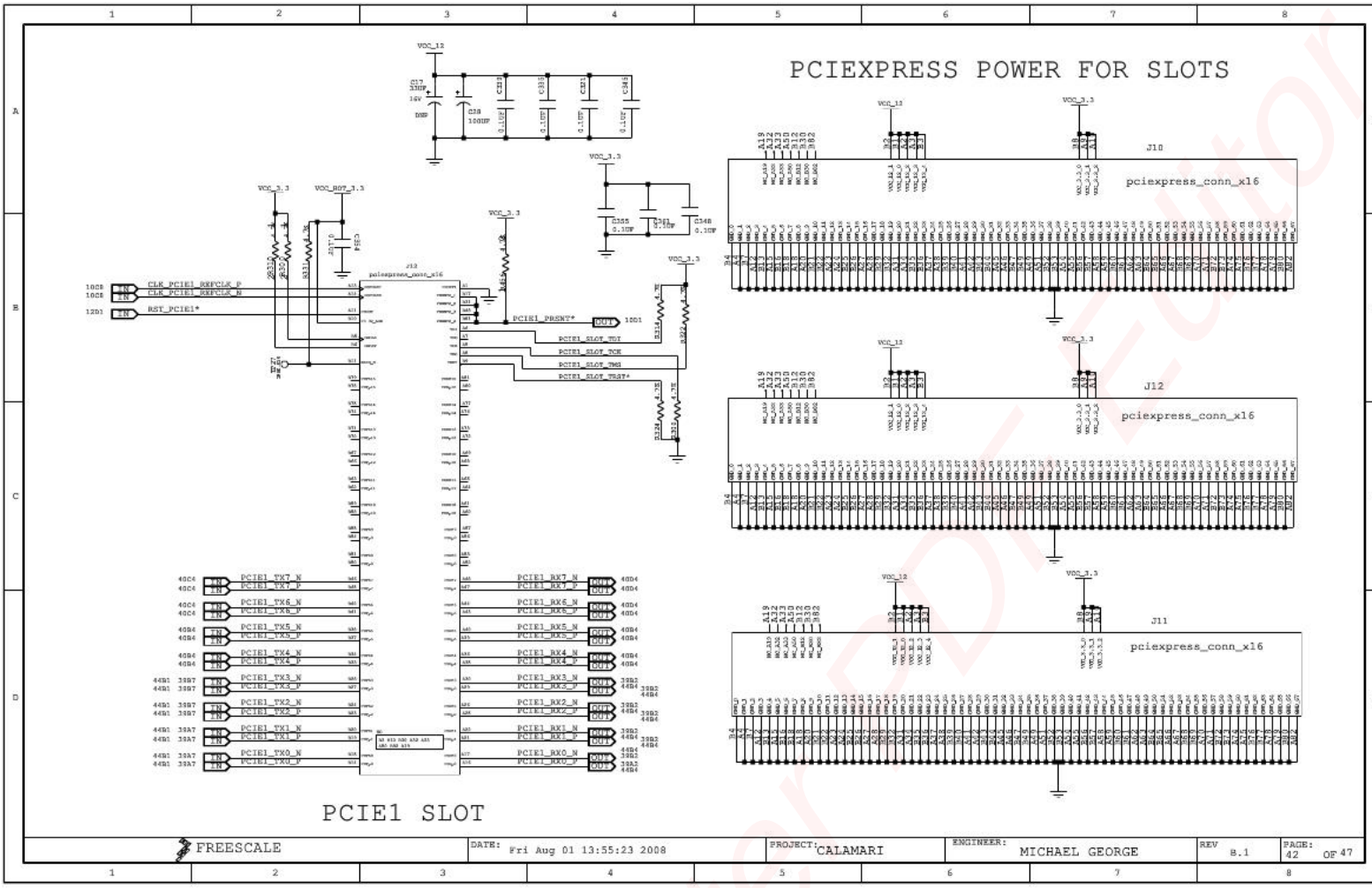


PCIE2 SLOT

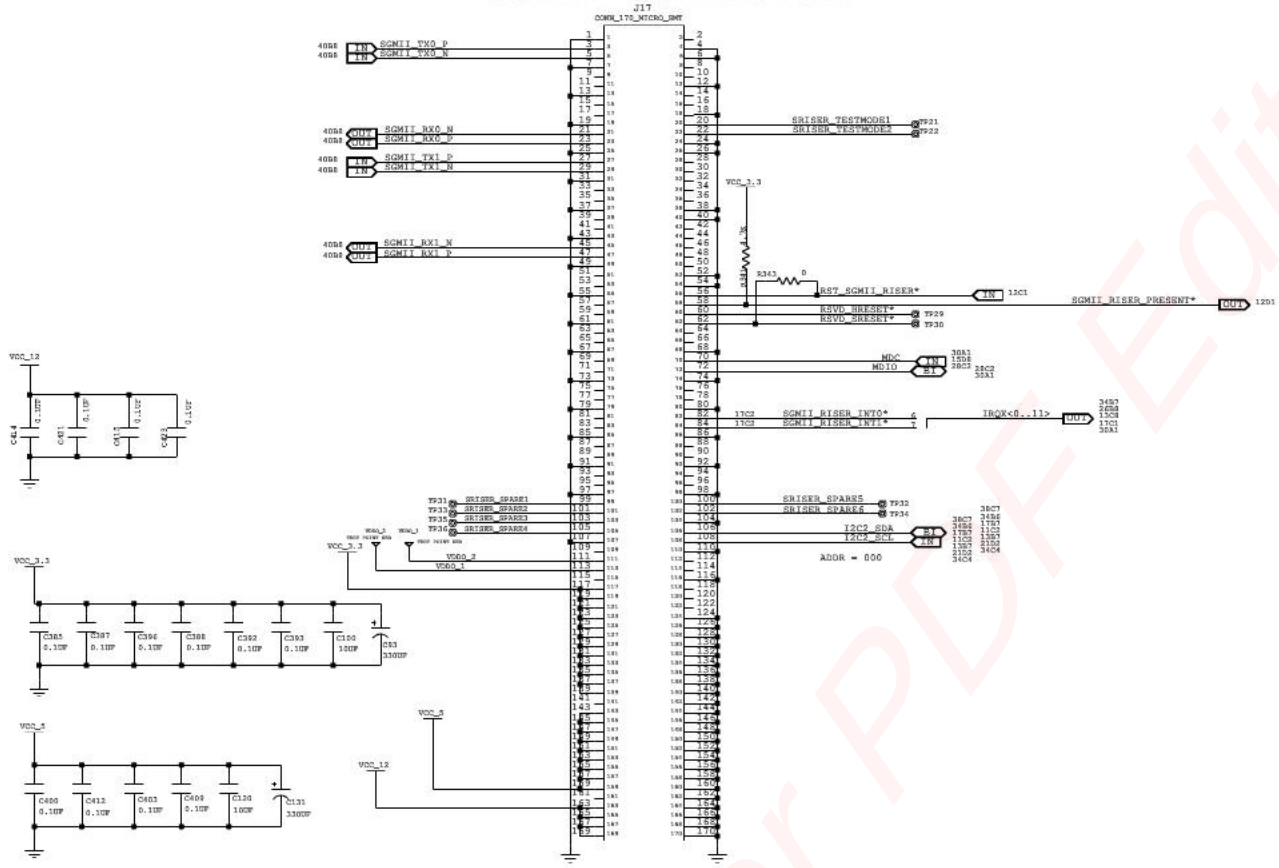


PCIE3 SLOT

FREESCALE	DATE: Fri Aug 01 13:55:05 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 41 OF 47

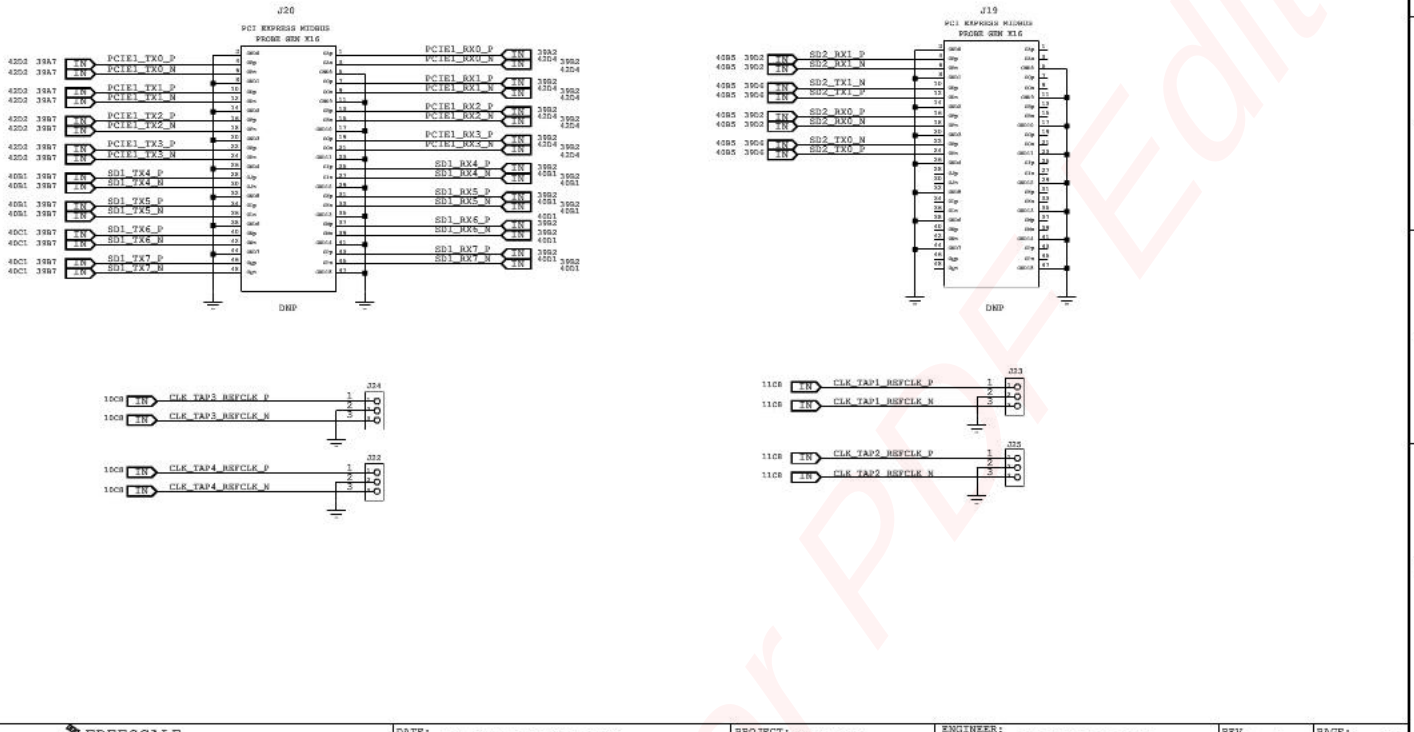


SGMII CONNECTOR



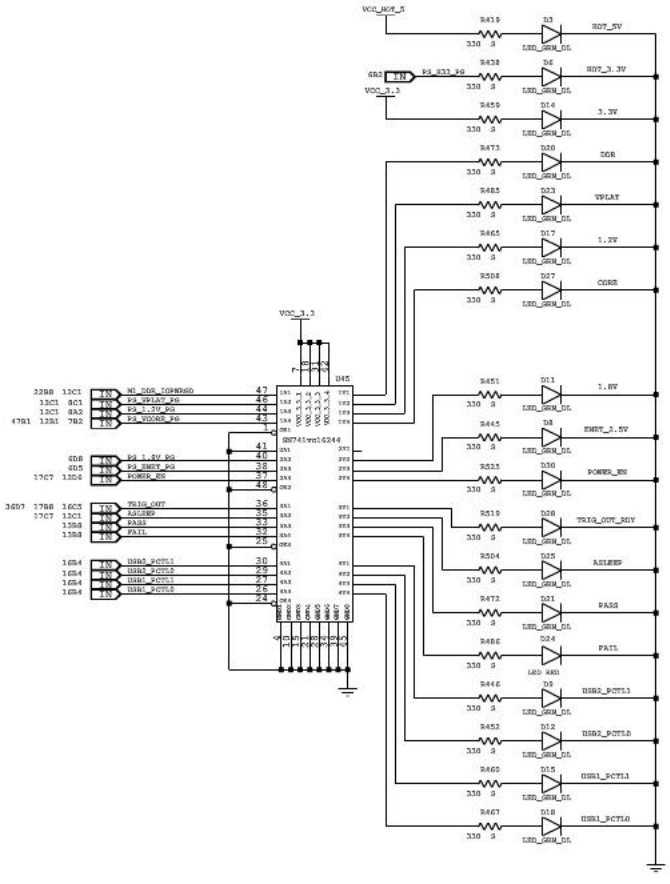
FREESCALE	DATE: Fri Aug 01 13:55:41 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 43 OF 47

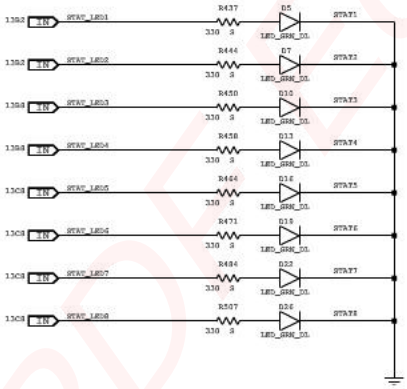
MIDBUS PROBE



FREESCALE	DATE: Fri Aug 01 13:55:59 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 44 OF 47

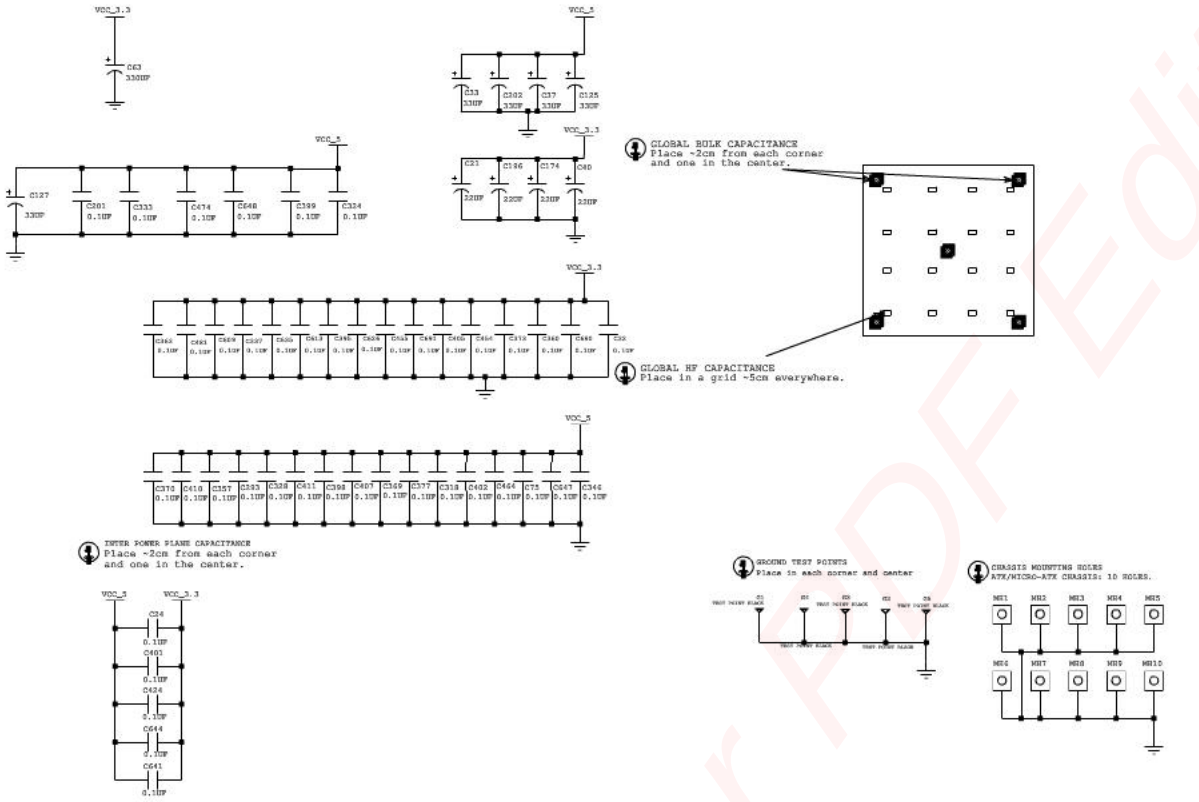
STATUS, POWER, DEBUG LEDS



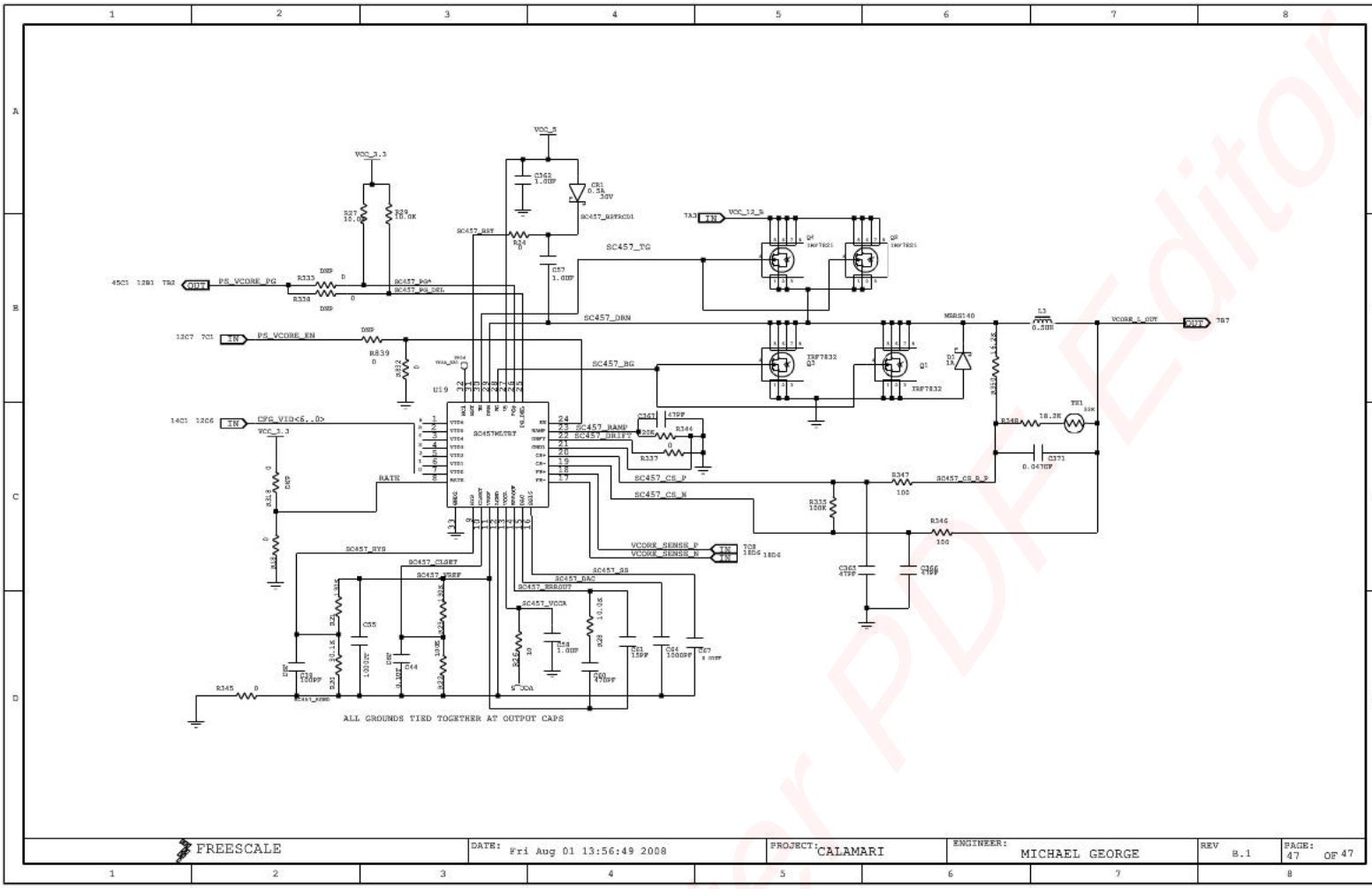


FREESCALE	DATE: Fri Aug 01 13:56:19 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 45 OF 47

GLOBAL BYPASS, MOUNTING, ETC



FREESCALE	DATE: Fri Aug 01 13:56:34 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 46 OF 47



FREESCALE	DATE: Fri Aug 01 13:56:49 2008	PROJECT: CALAMARI	ENGINEER: MICHAEL GEORGE	REV B.1	PAGE: 47 OF 47