T1040RDB

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Version Control

Version	Date	Modifications
V0.1	2013/06	First release of Schematics
V1.0	2013/10	Released to Manufacturing
V2.0	2014/01	Add SD_REFCLK1_SEL to select SerDes PLL1 input clock frequency Change the direction of the battery holder

Variants	Description
INTERPOSER	INTERPOSER version (normal + VIT)
T1040/T2081 RDB	T1040RDB version (normal + VNIT)

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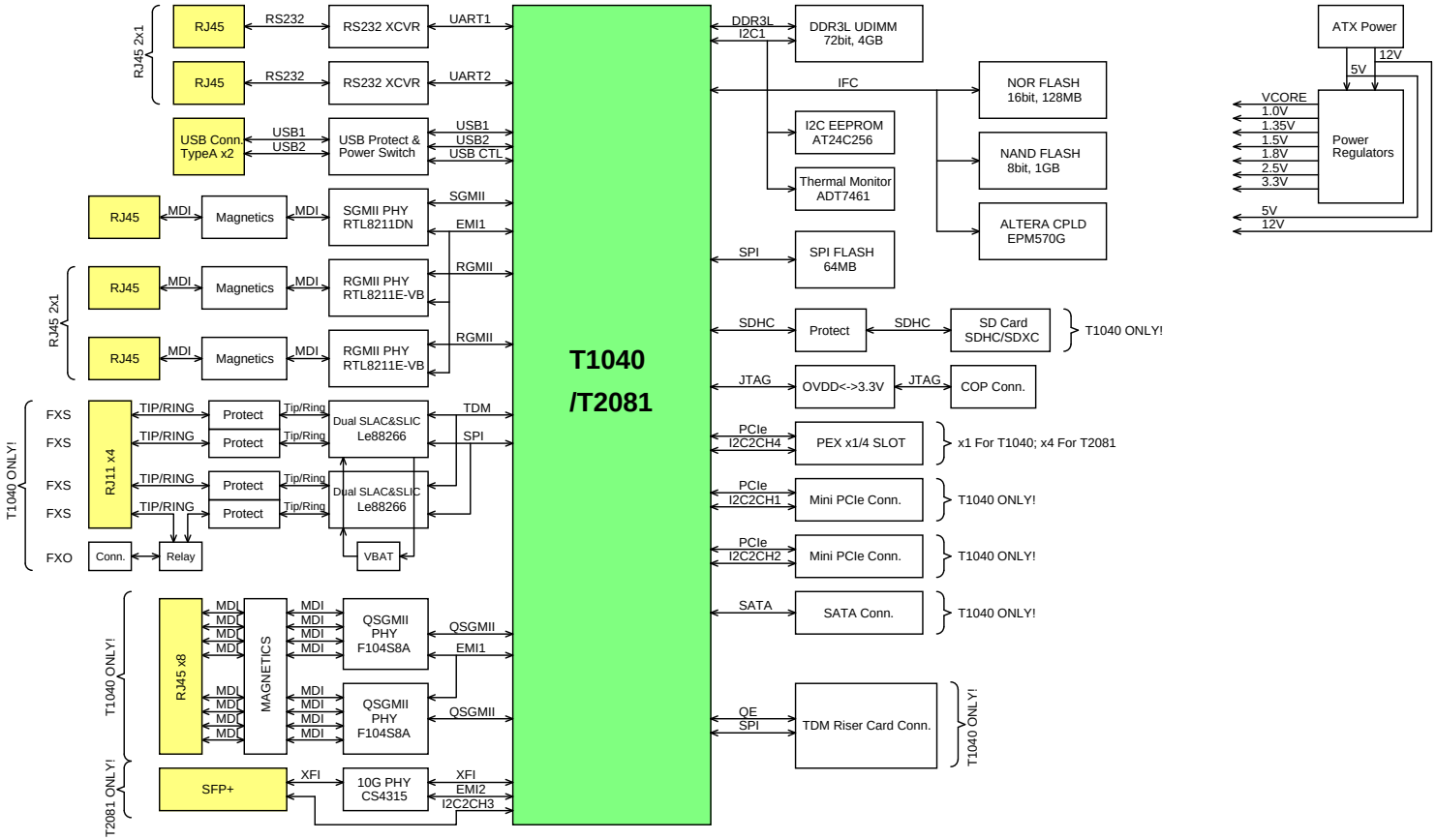
SYSTEM BLOCK DIAGRAM



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T1040 DDR3L MEMORY INTERFACE

1.35V DDR3L SDRAM UDIMM
4GB (x72, ECC, DR)

Micron MPN(4GB,1600): MT18KSF51272AZ-1G6
Micron MPN(2GB,2133): MT9JSF25672AZ-2G1

U1A
DDR CONTROLLER
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T1040

J1A
DDR3_DIMM

J1B
DDR3_DIMM

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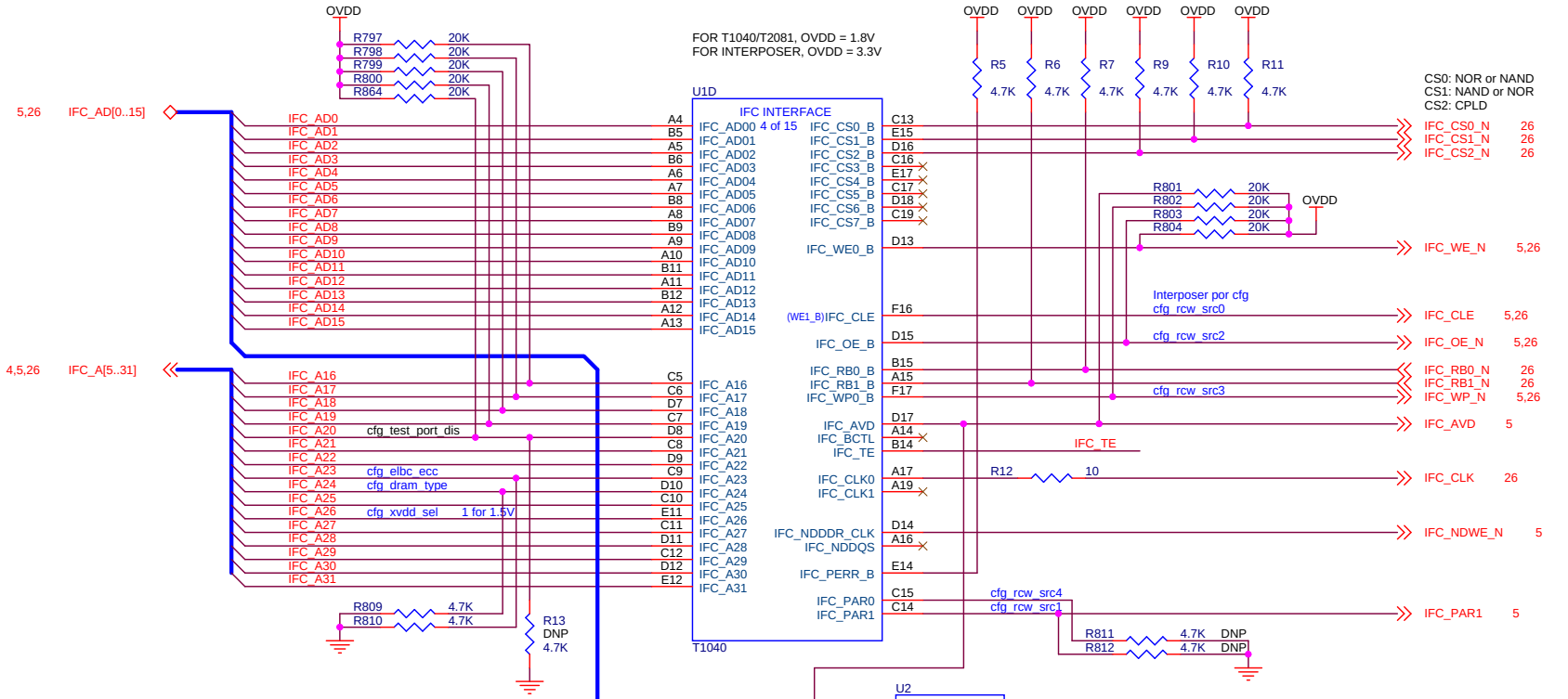
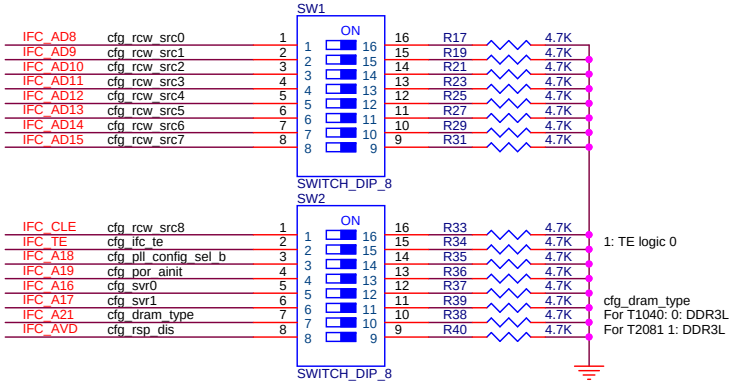
T1040 IFC INTERFACE



T1040 RESET CONFIGURATION

cfg_rcw_src[0:8]
0_0010_0111: NOR FLASH BOOT
0_0100_0000: SD CARD BOOT
0_0100_0101: SPI BOOT
1_0001_1001: NAND FLASH BOOT



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T1040 NOR and NAND FLASH INTERFACE

FOR T1040/T2081, OVDD = 1.8V
FOR INTERPOSER, OVDD = 3.3V

128MB 16-BIT NOR FLASH

U4 — JS28F00AM29EWHA

1GB 8-BIT NAND FLASH

U6 — MT29F8G08ABABAWP-ITX:B

On Interposer ONLY, NAND AVD is routed on PAR1

On Interposer, NAND MPN: K9F5608U0D

U98, U99 — TXBN0304RSV

U7, U11 — TXBN0304RSV

U8, U9, U10 — 74LVC1G86

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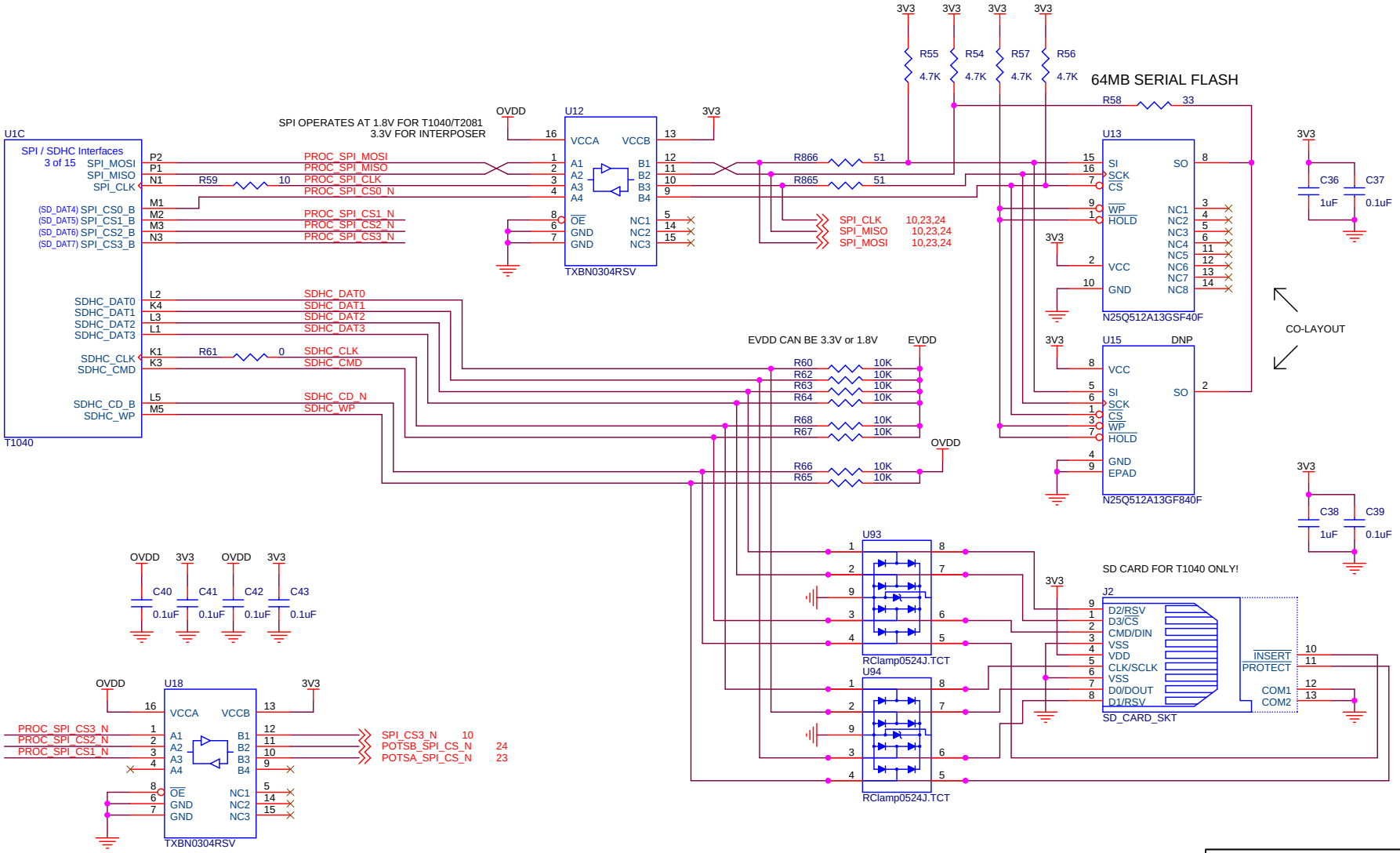
T1040 SPI FLASH and SDHC INTERFACE



Title: T1040RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
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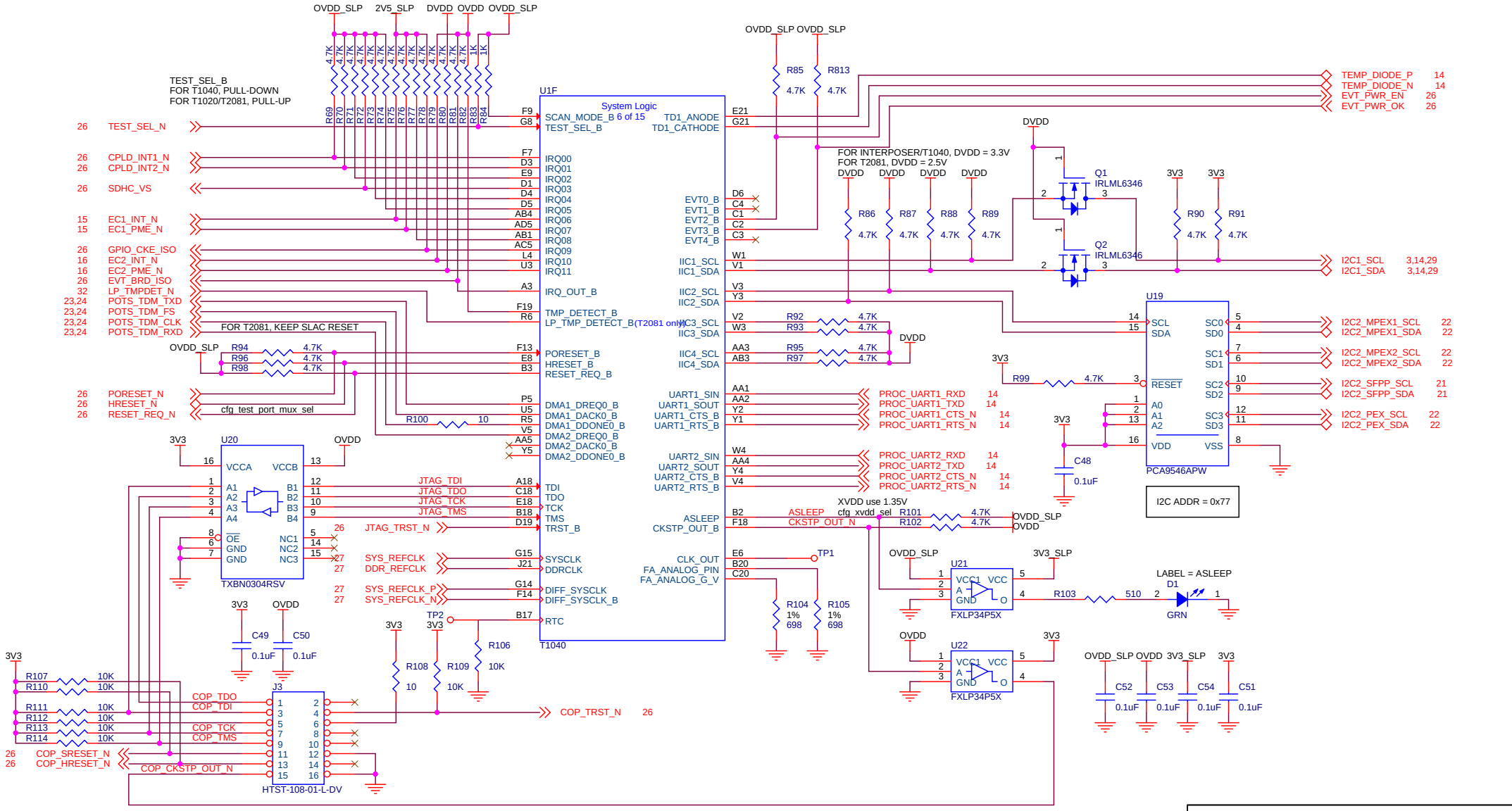
T1040 SYSTEM LOGIC INTERFACE



Title: T1040RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
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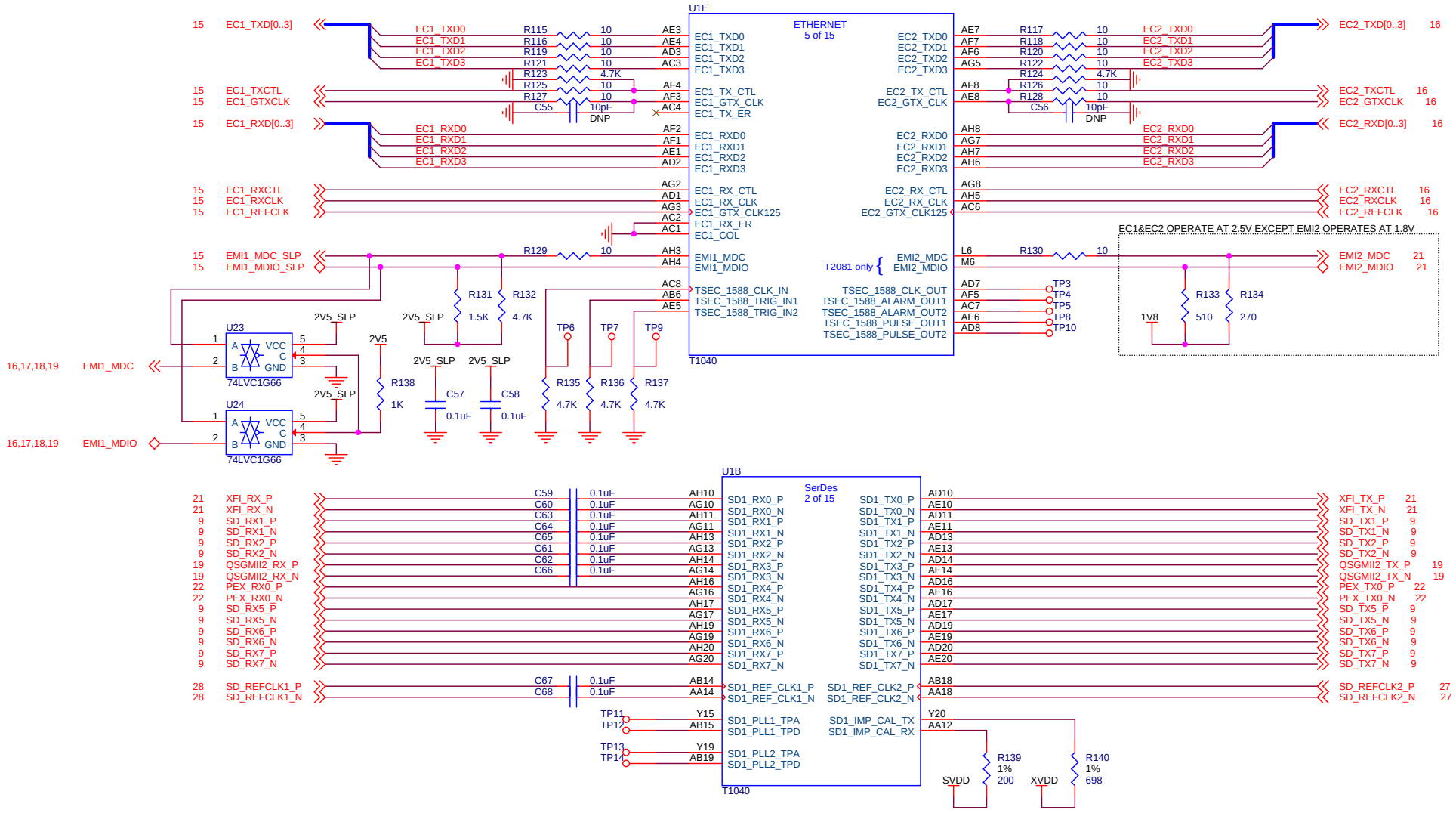
T1040 ETHERNET and SERDES INTERFACE



Title: T1040RDB			
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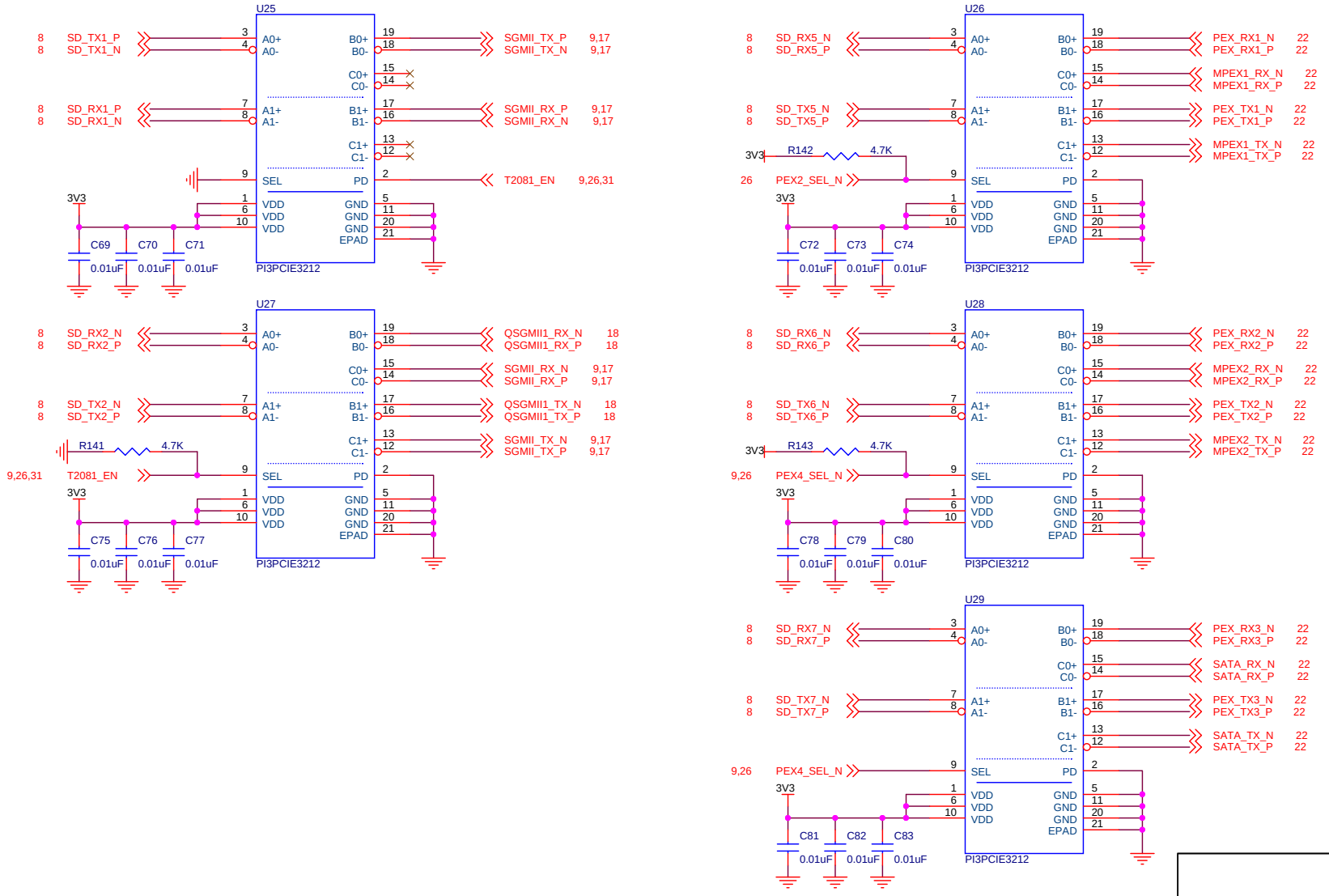
SERDES MUX/DEMUX SWITCHs



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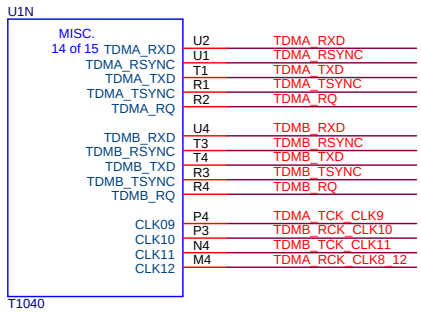
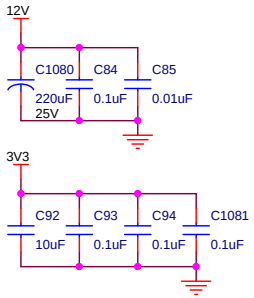
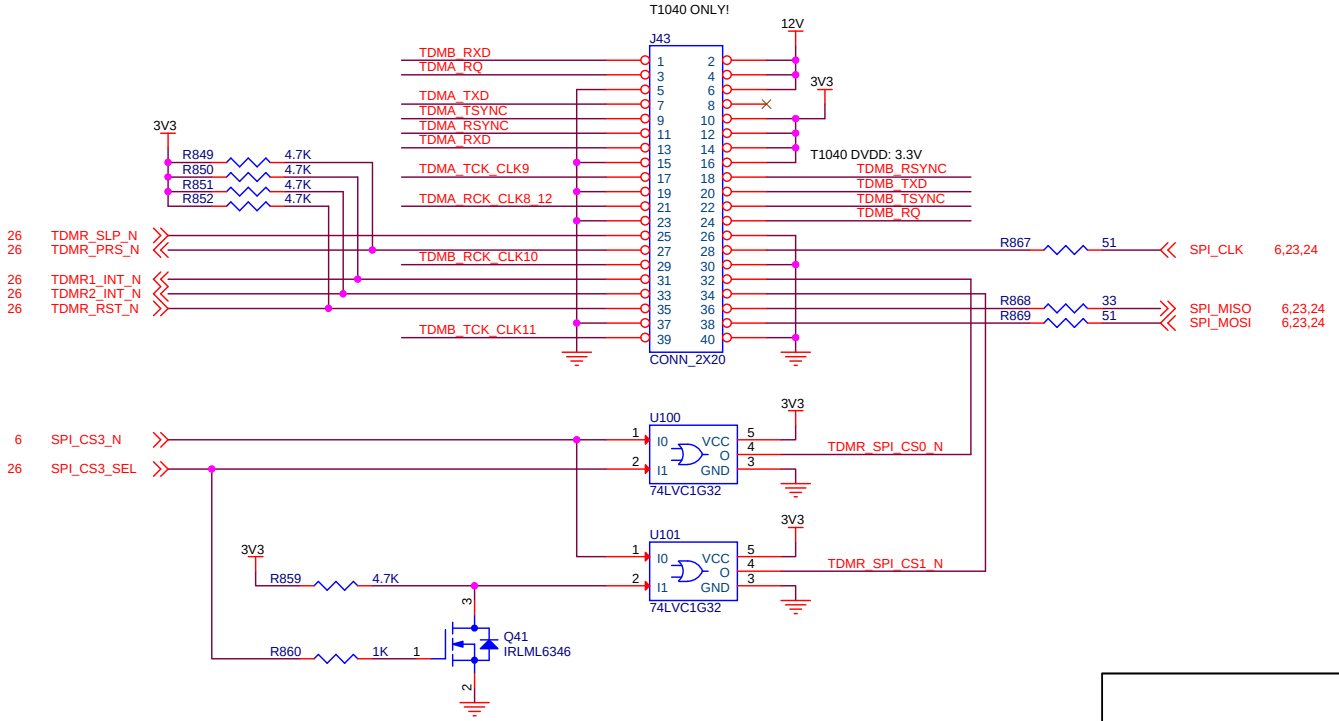
T1040 QE INTERFACE





TDM RISER CARD CONNECTOR



Title: T1040RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
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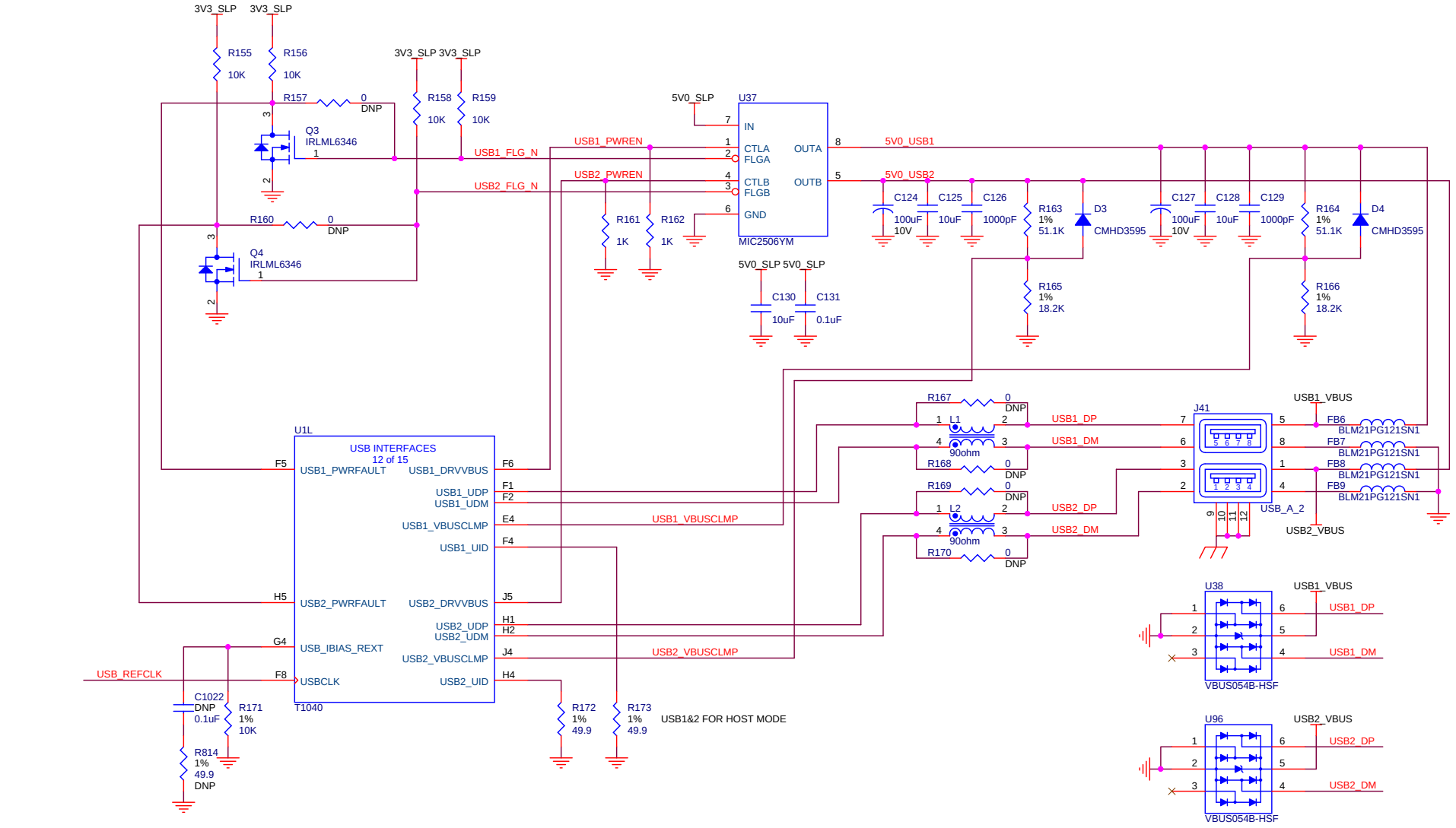
T1040 USB INTERFACE



Title: T1040RDB			
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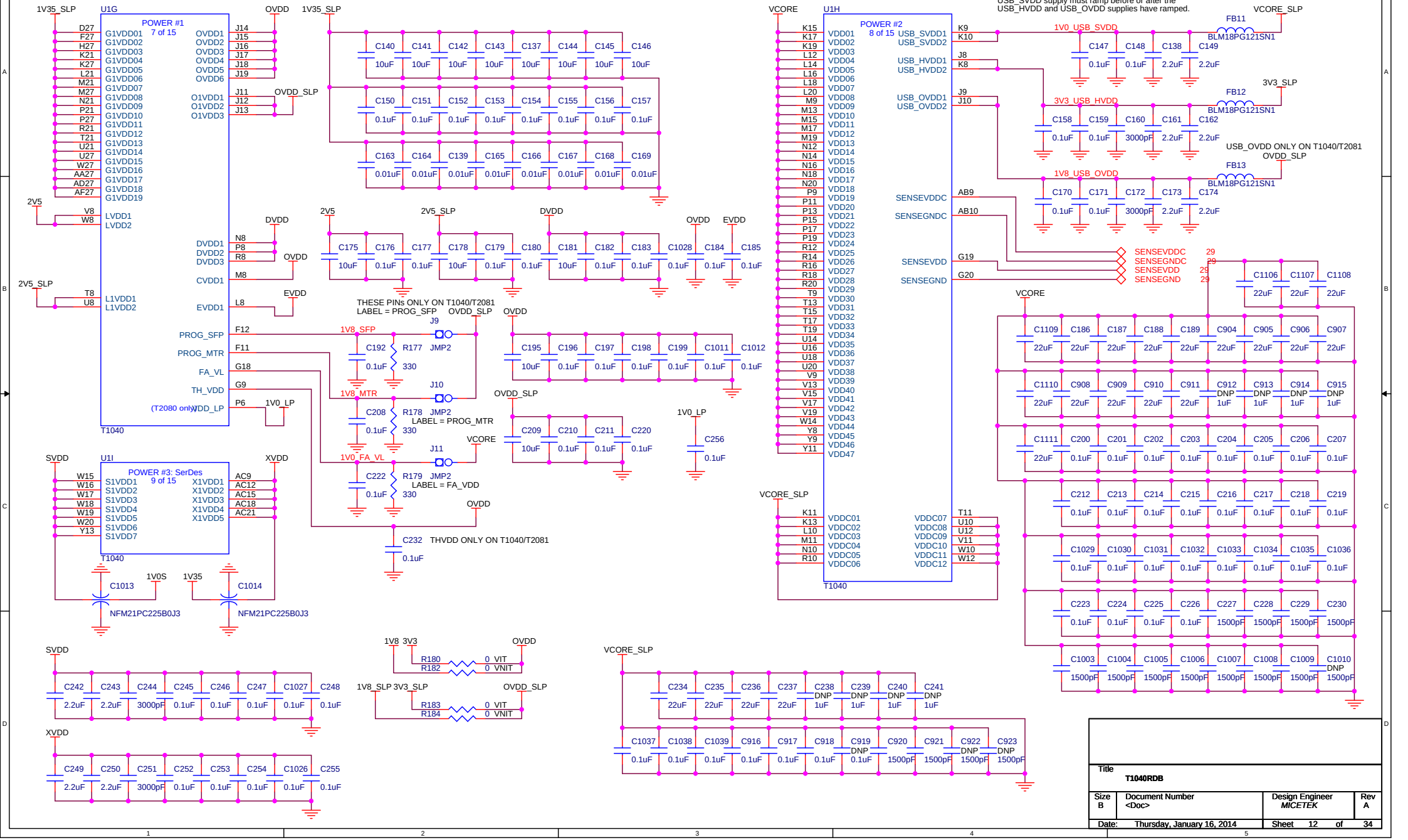
T1040 POWER SUPPLY



Title: T1040RDB			
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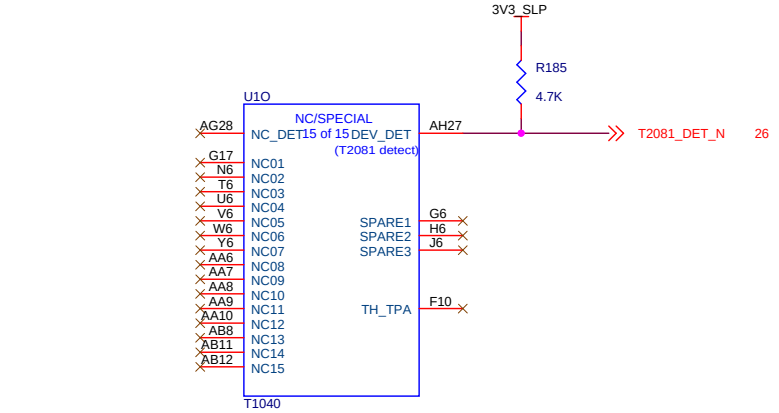
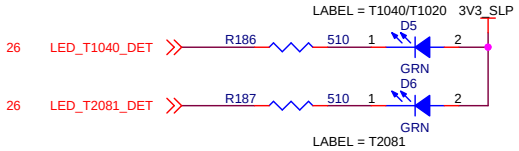
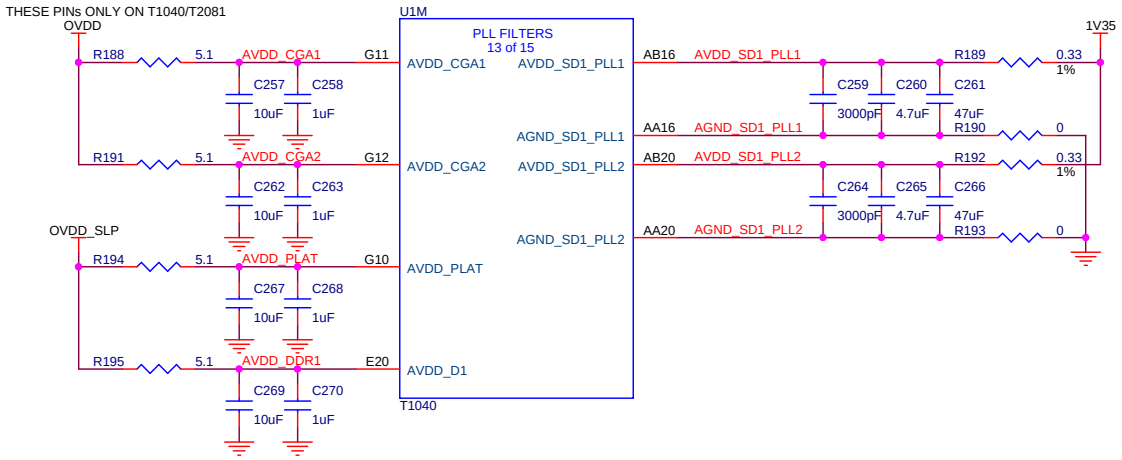
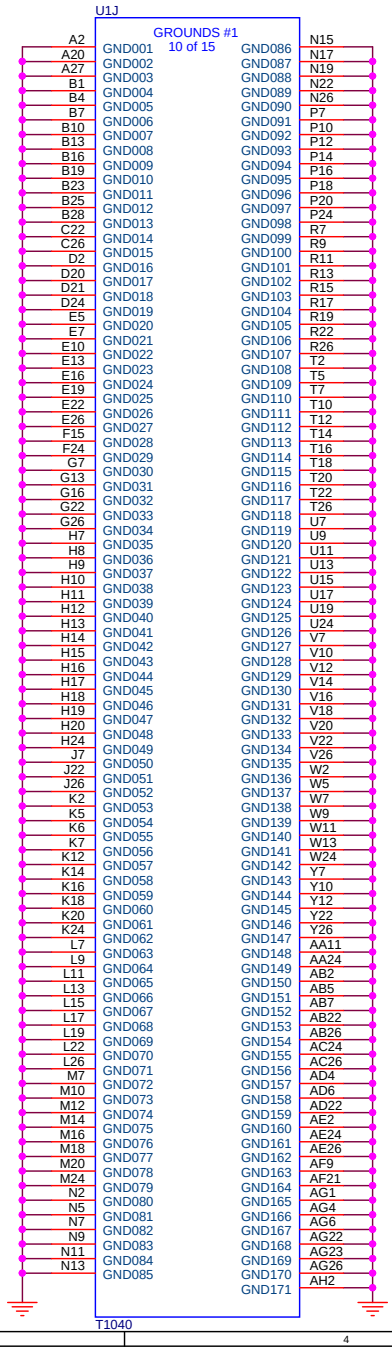
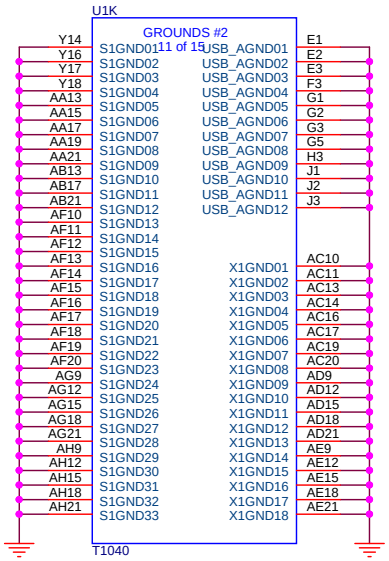
T1040 PLL FILTERs and GROUND











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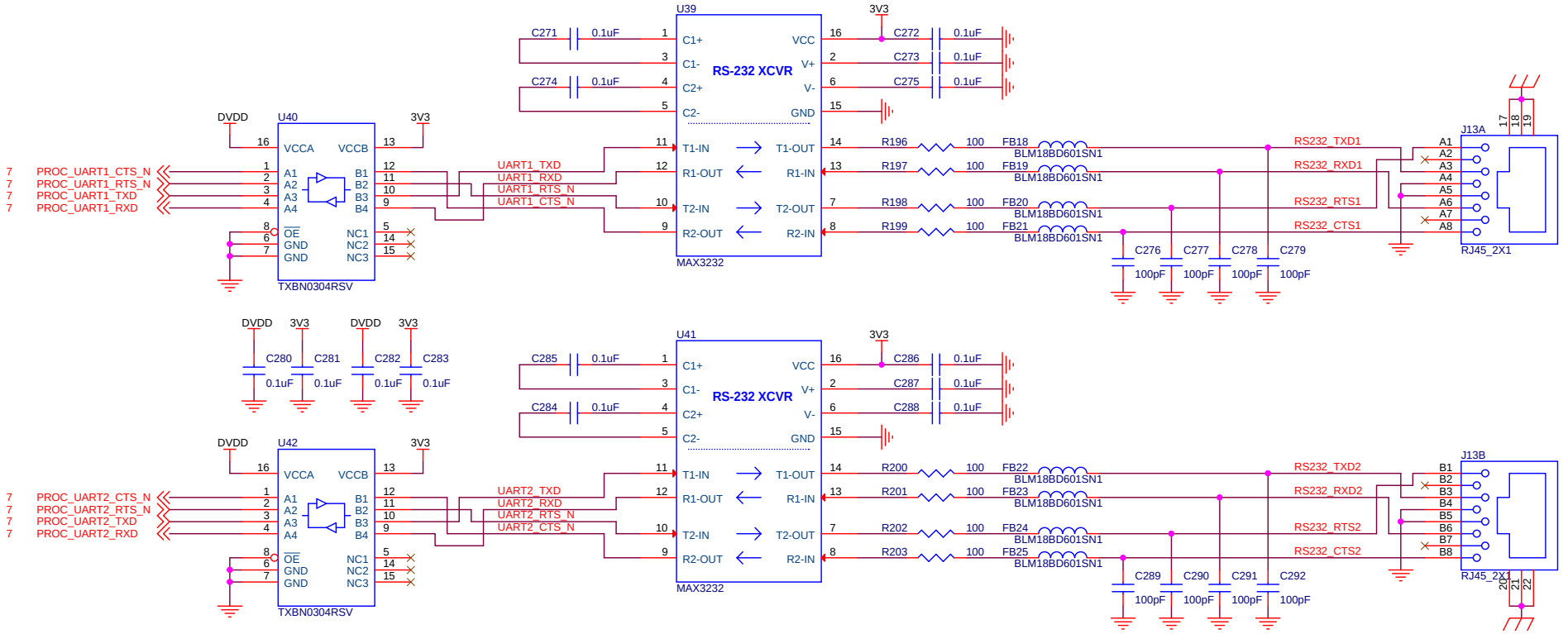
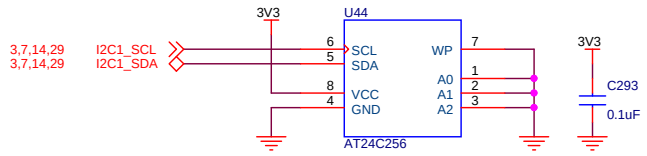
T1040 DUART and I2C DEVICE INTERFACE



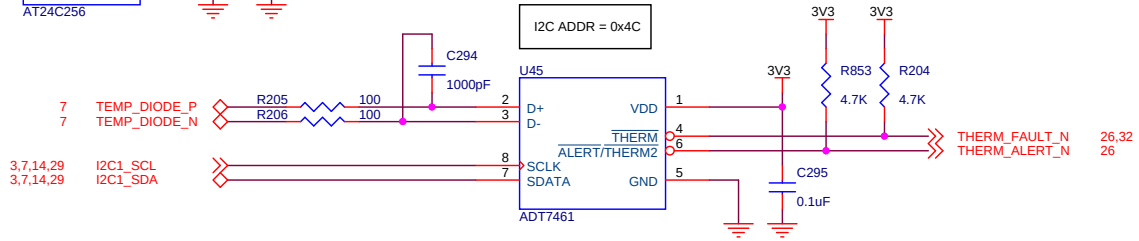
I2C EEPROM

I2C ADDR = 0x50

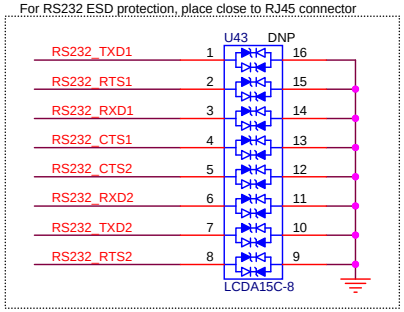


I2C THERMAL MONITOR

I2C ADDR = 0x4C



For RS232 ESD protection, place close to RJ45 connector



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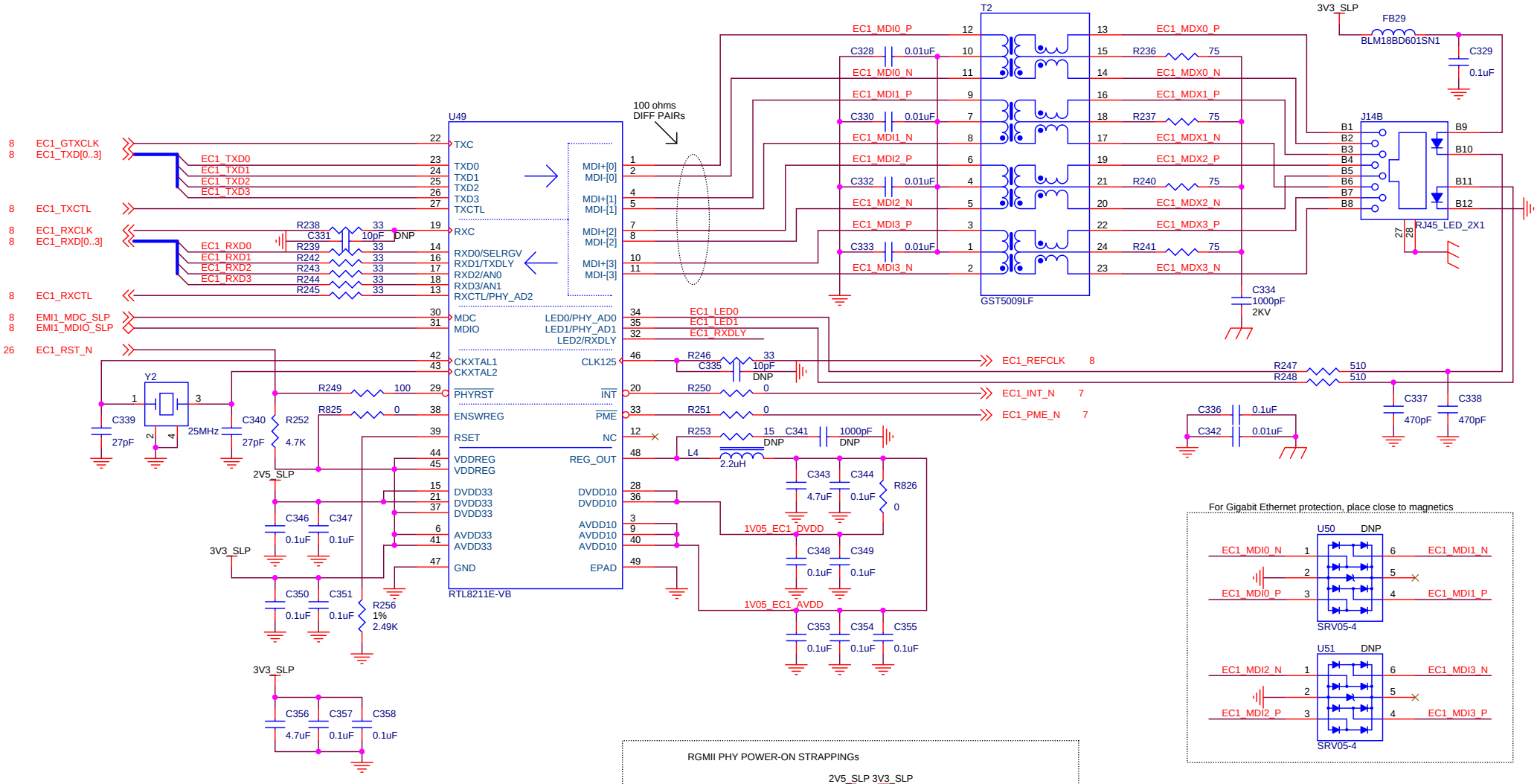
RGMII ETHERNET PORT 1



Title: T1040RDB			
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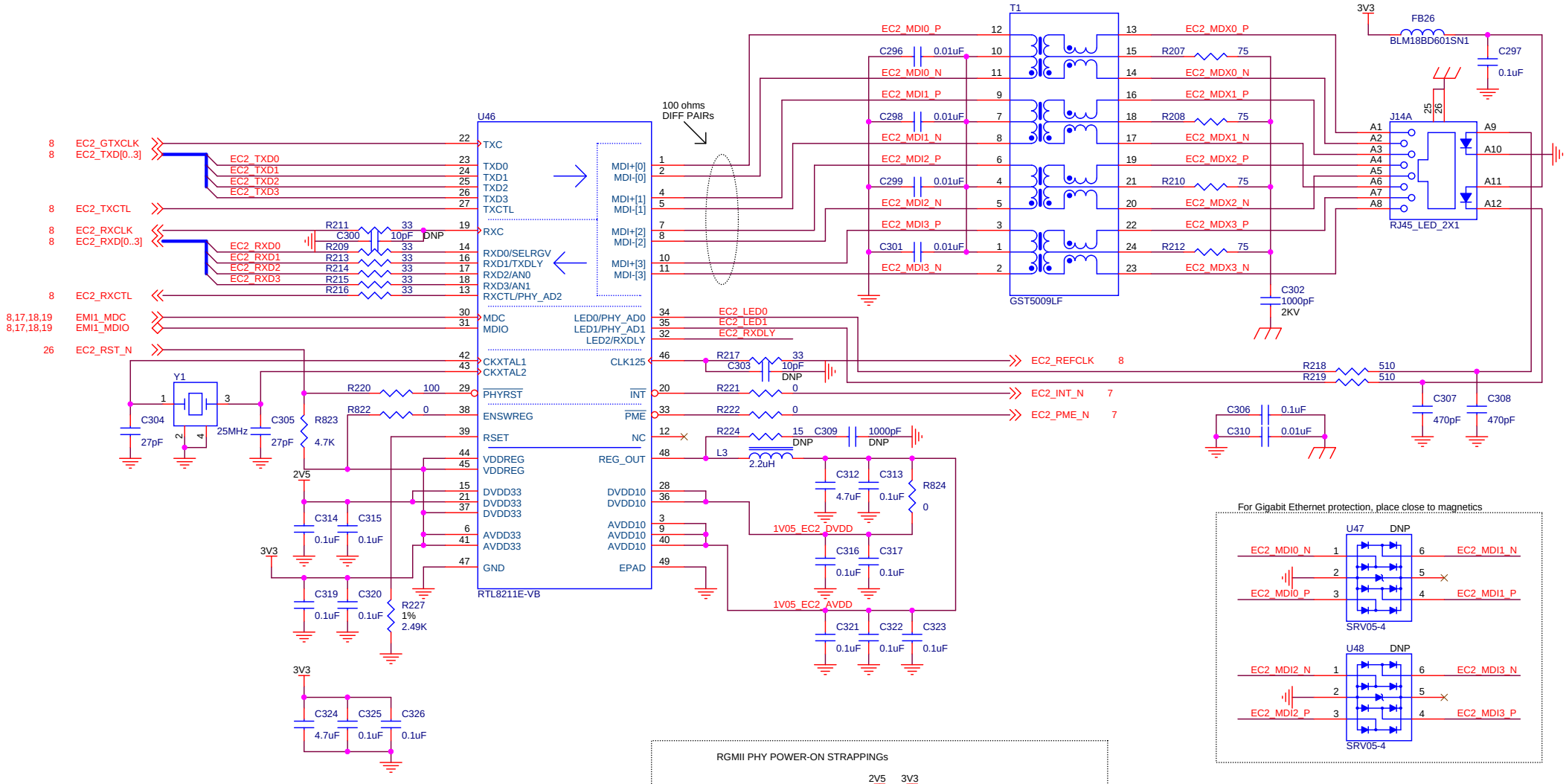
RGMII ETHERNET PORT 2



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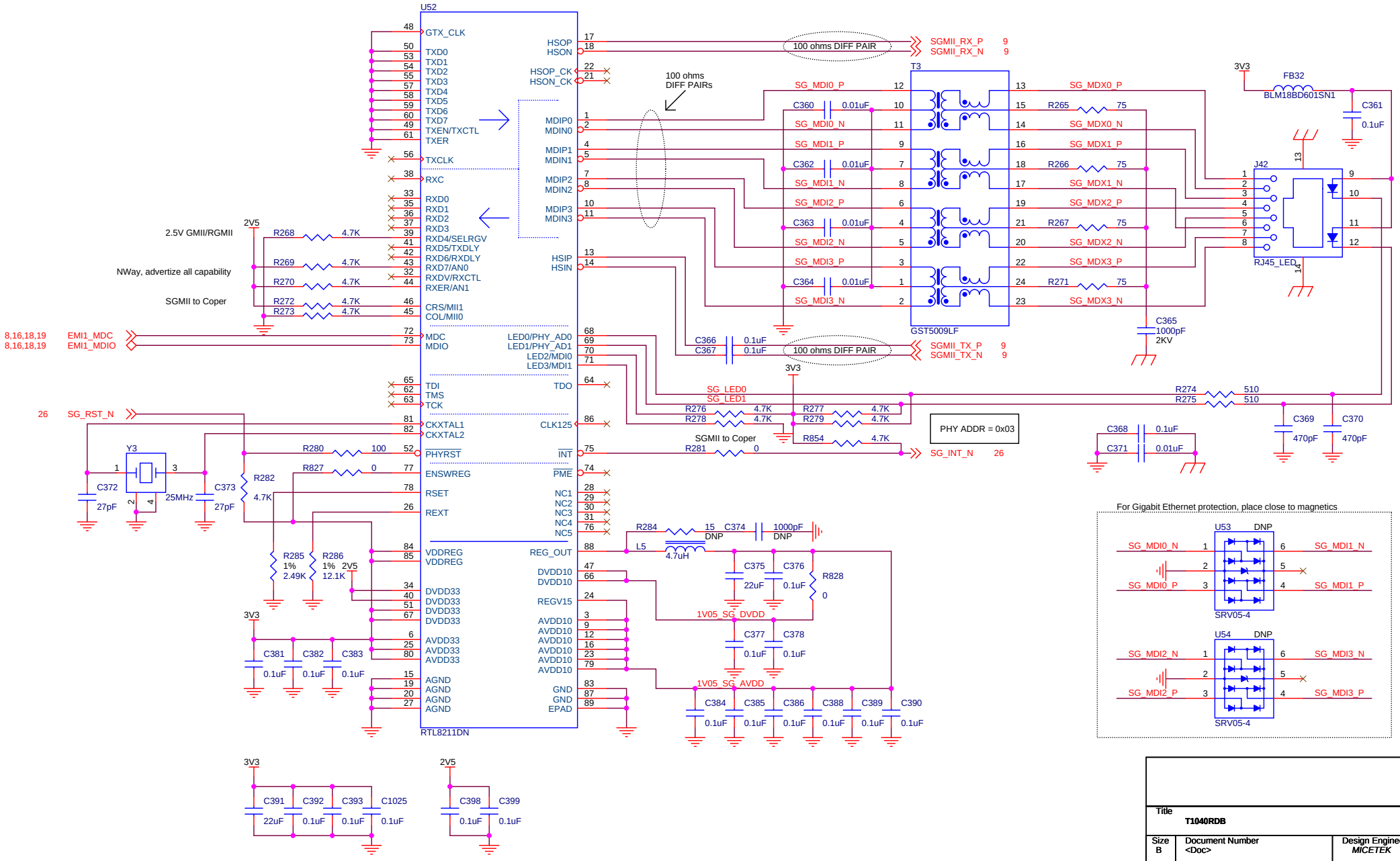
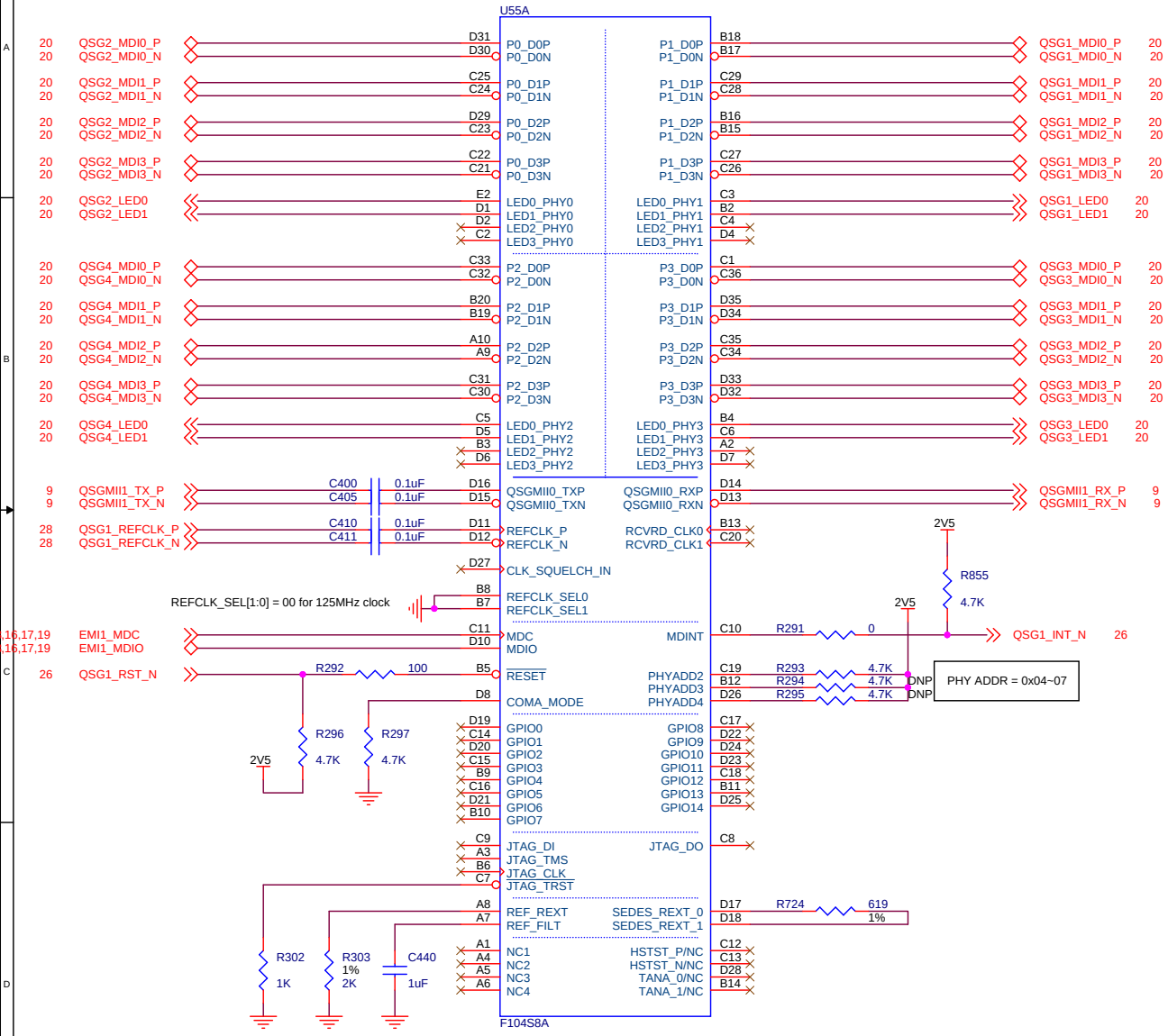
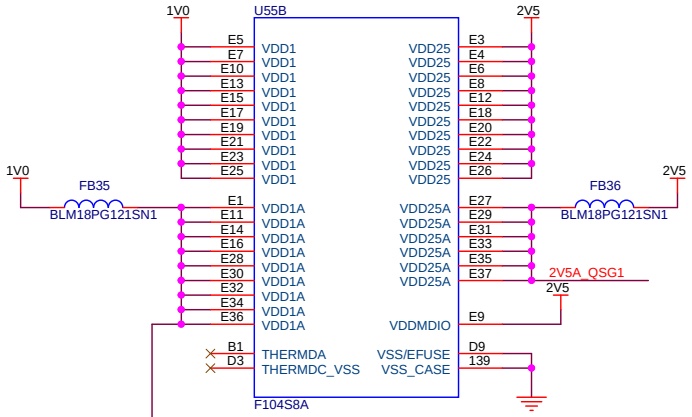
SGMII ETHERNET PORT

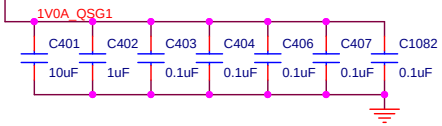


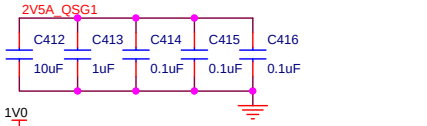
QSGMII PHY 1

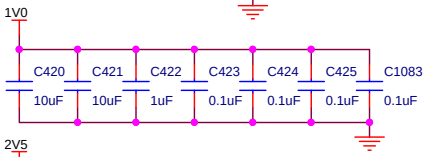
T1040 ONLY!

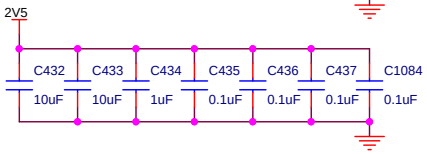












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QSGMII PHY 2

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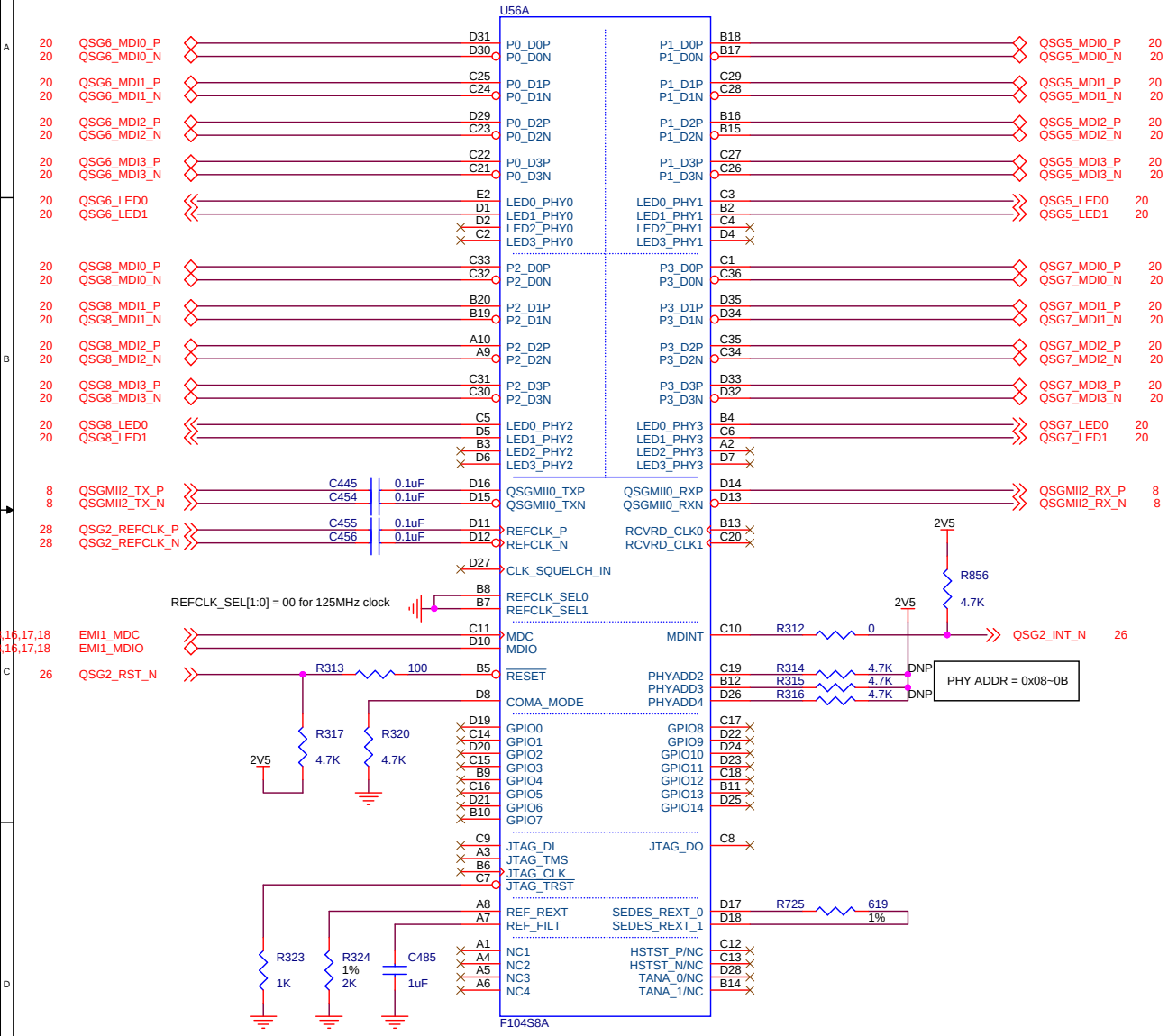

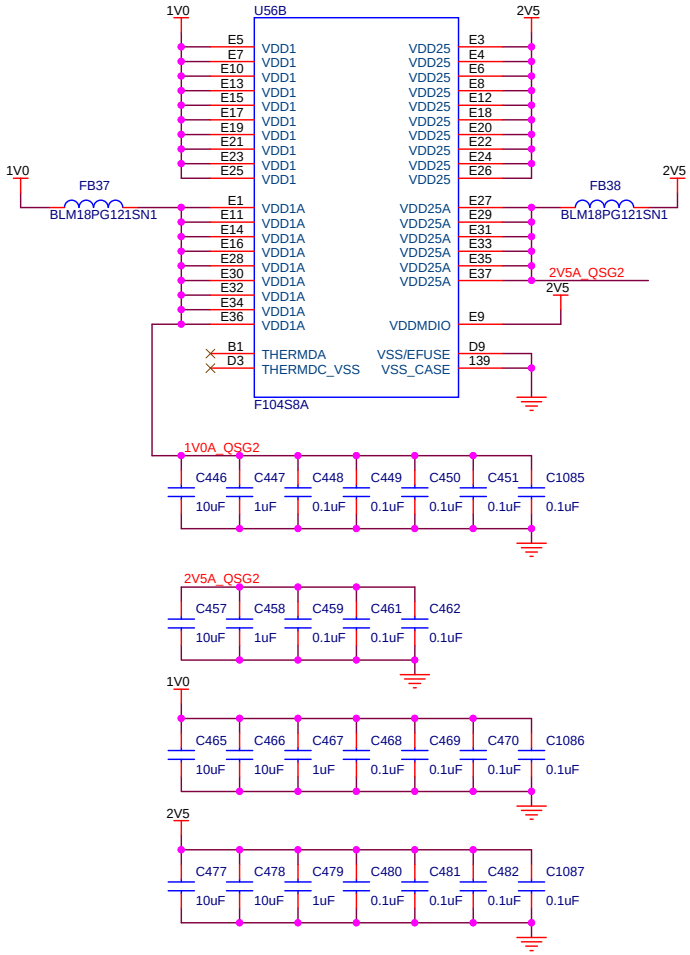

Title: T1040RDB			
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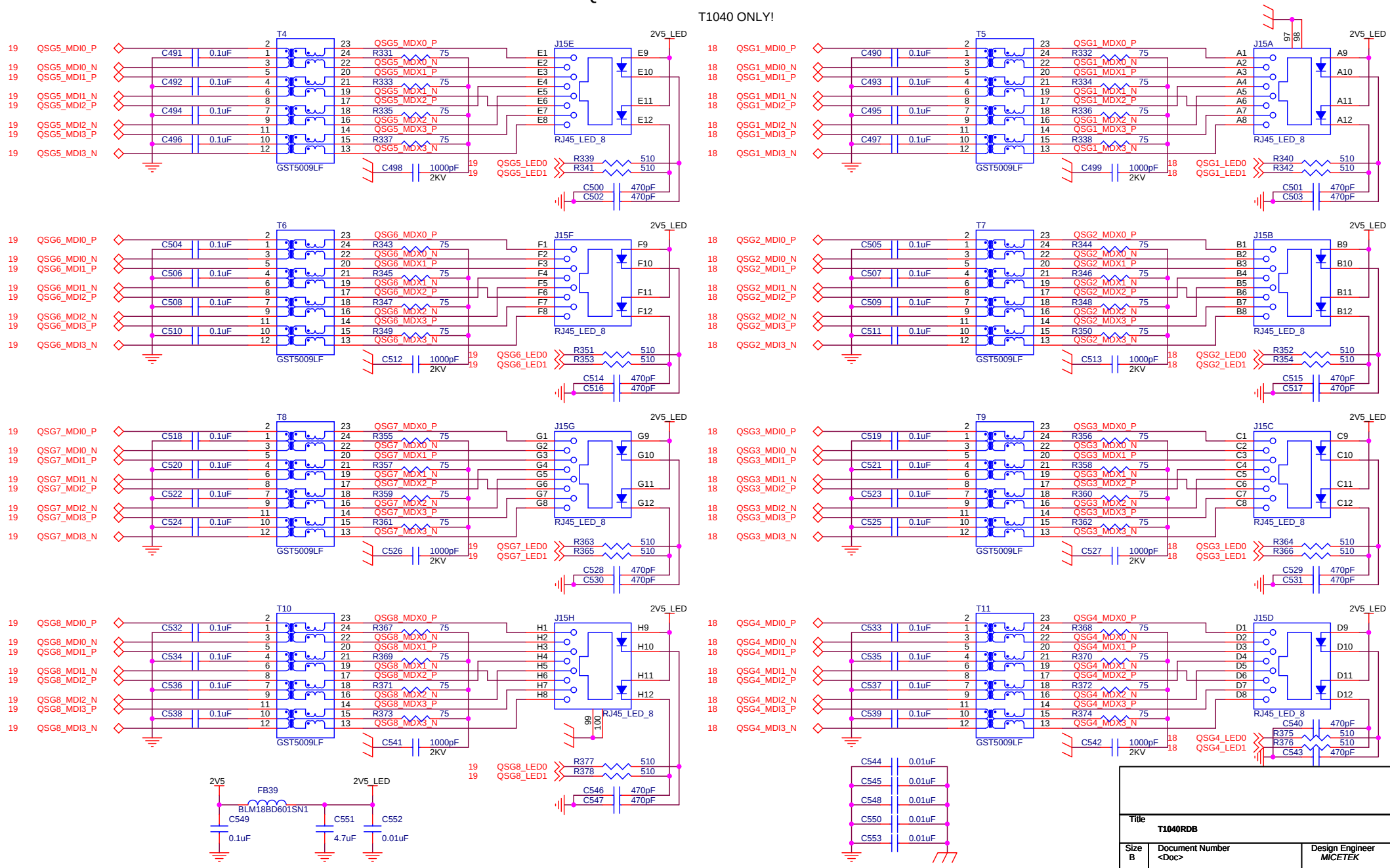
QSGMII ETHERNET PORTs

T1040 ONLY!



Title: T1040RDB			
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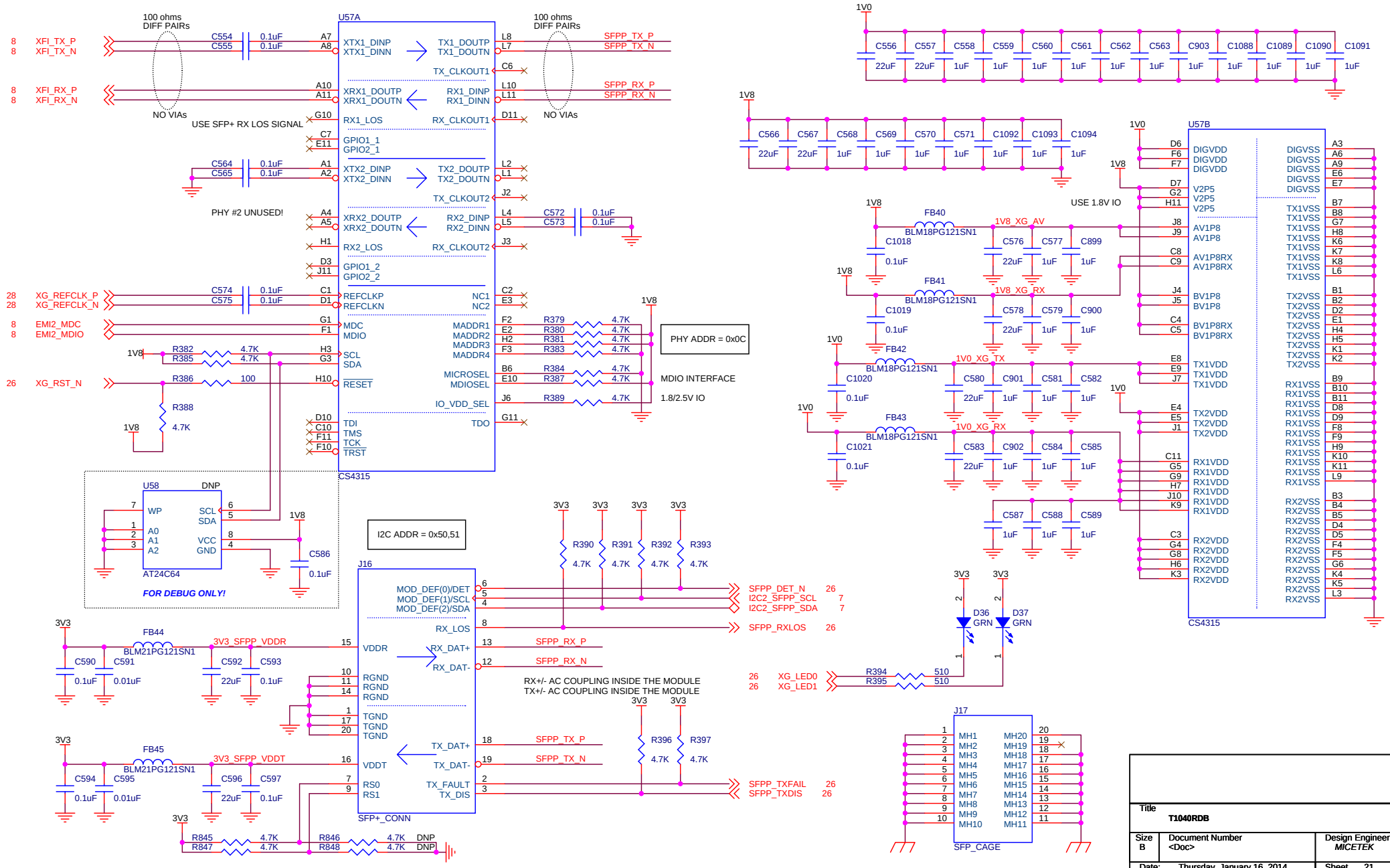
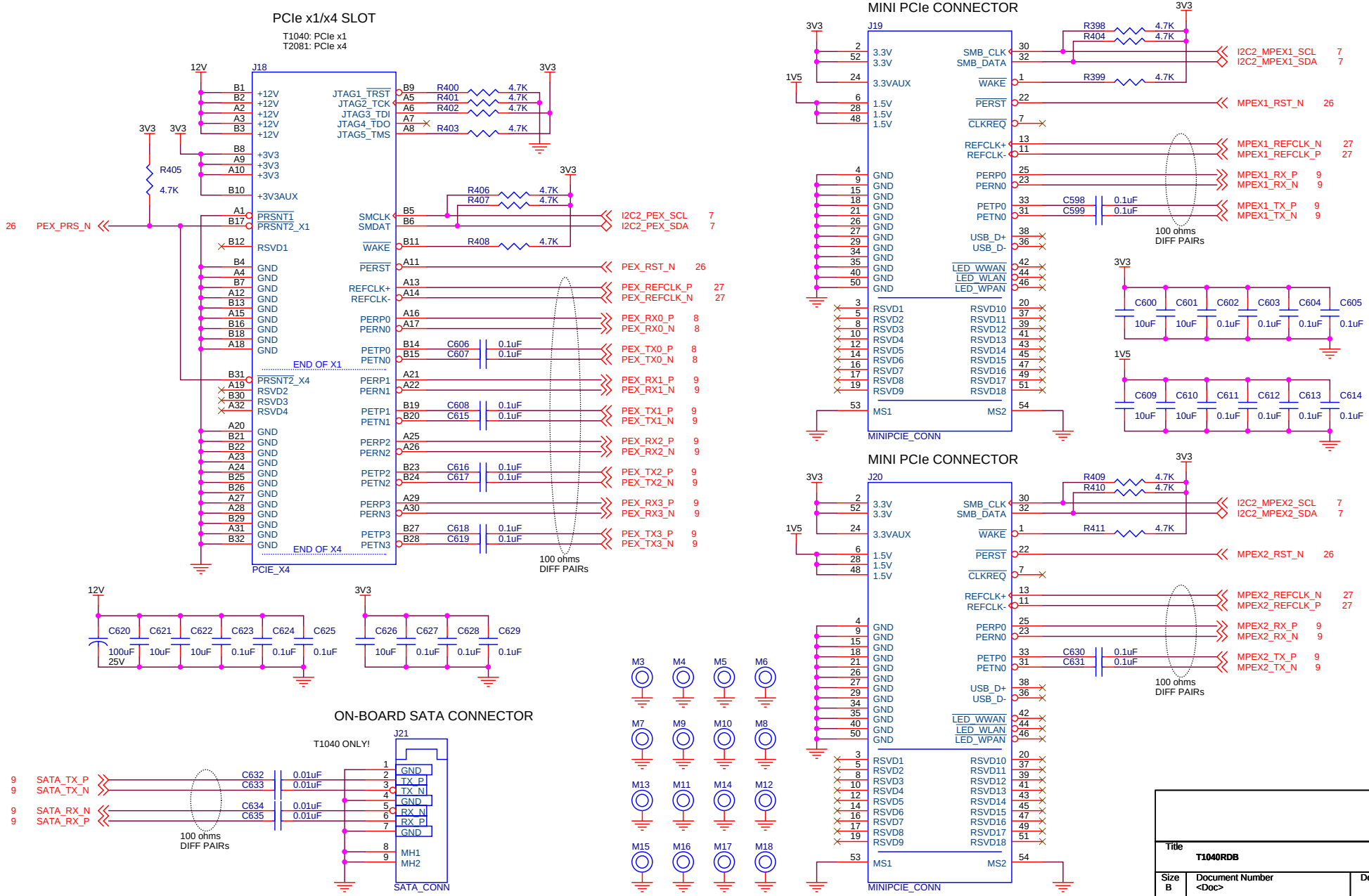
10G EDC PHY and SFP+ CONNECTOR

T2081 ONLY!



PCIe X1/X4 SLOT, MINI PCIe and SATA CONNECTORs



Title: T1040RDB			
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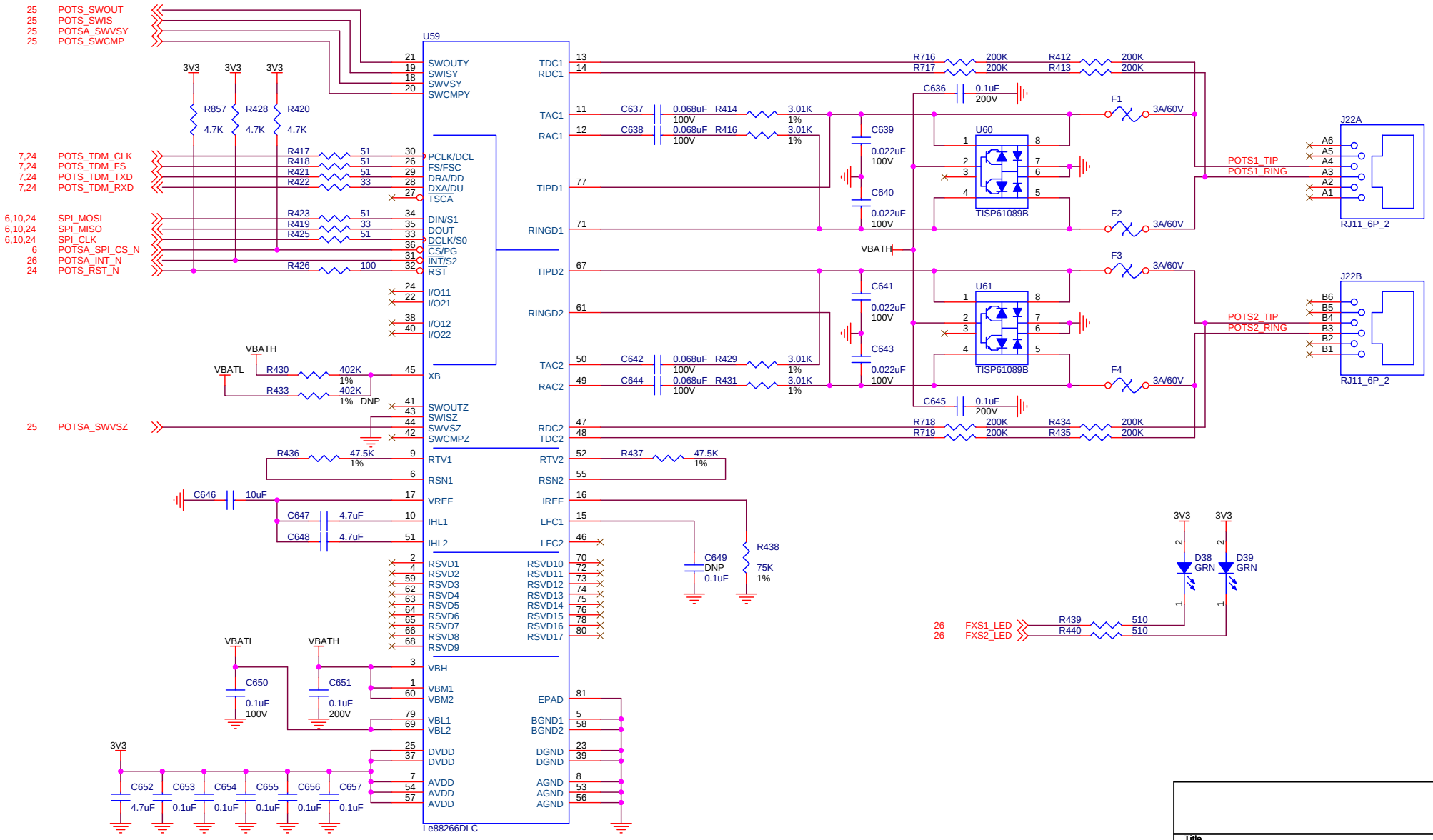
POTS 1&2 INTERFACE

T1040 ONLY!



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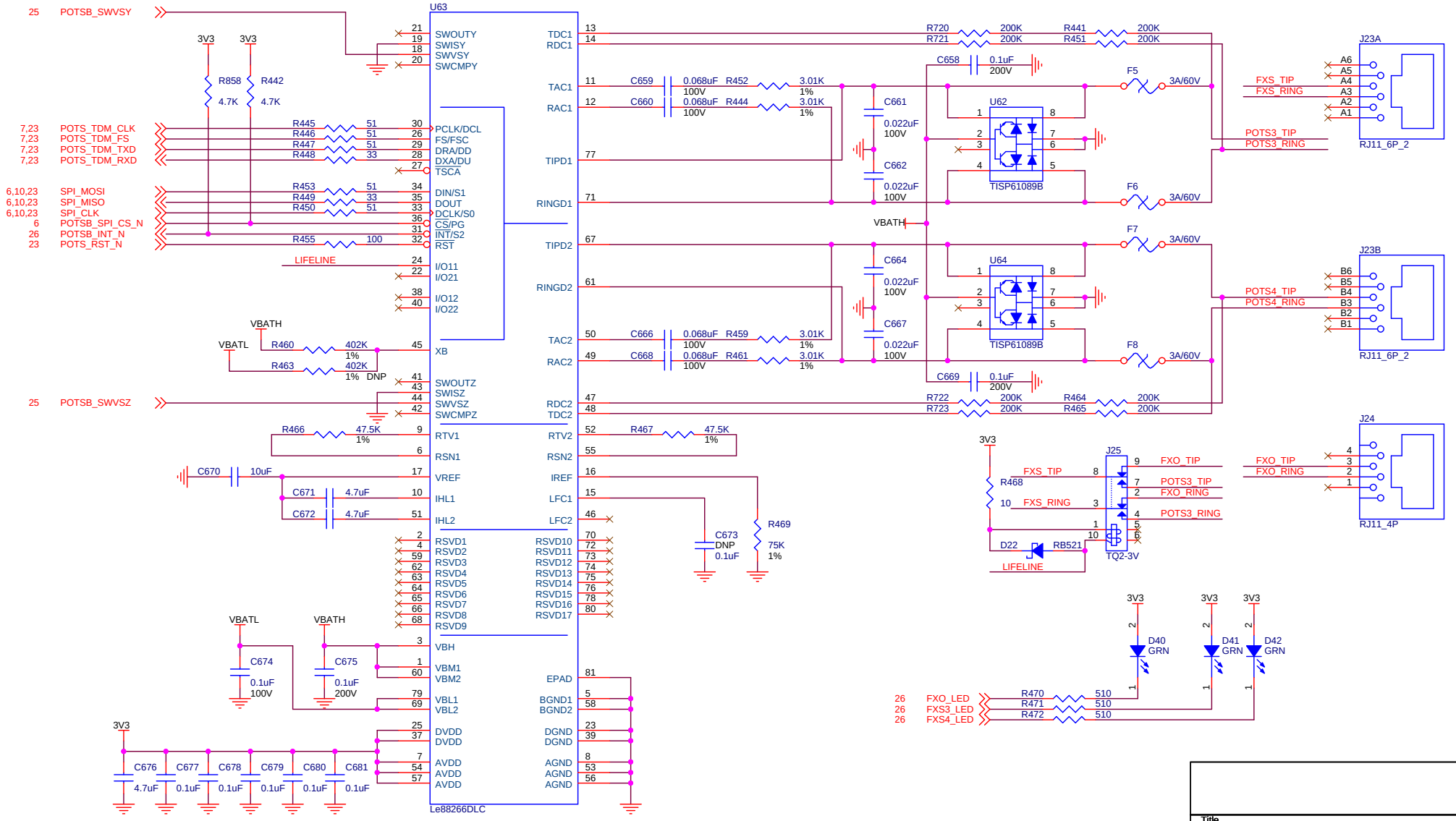
POTS 3&4 INTERFACE

T1040 ONLY!



Title: T1040RDB			
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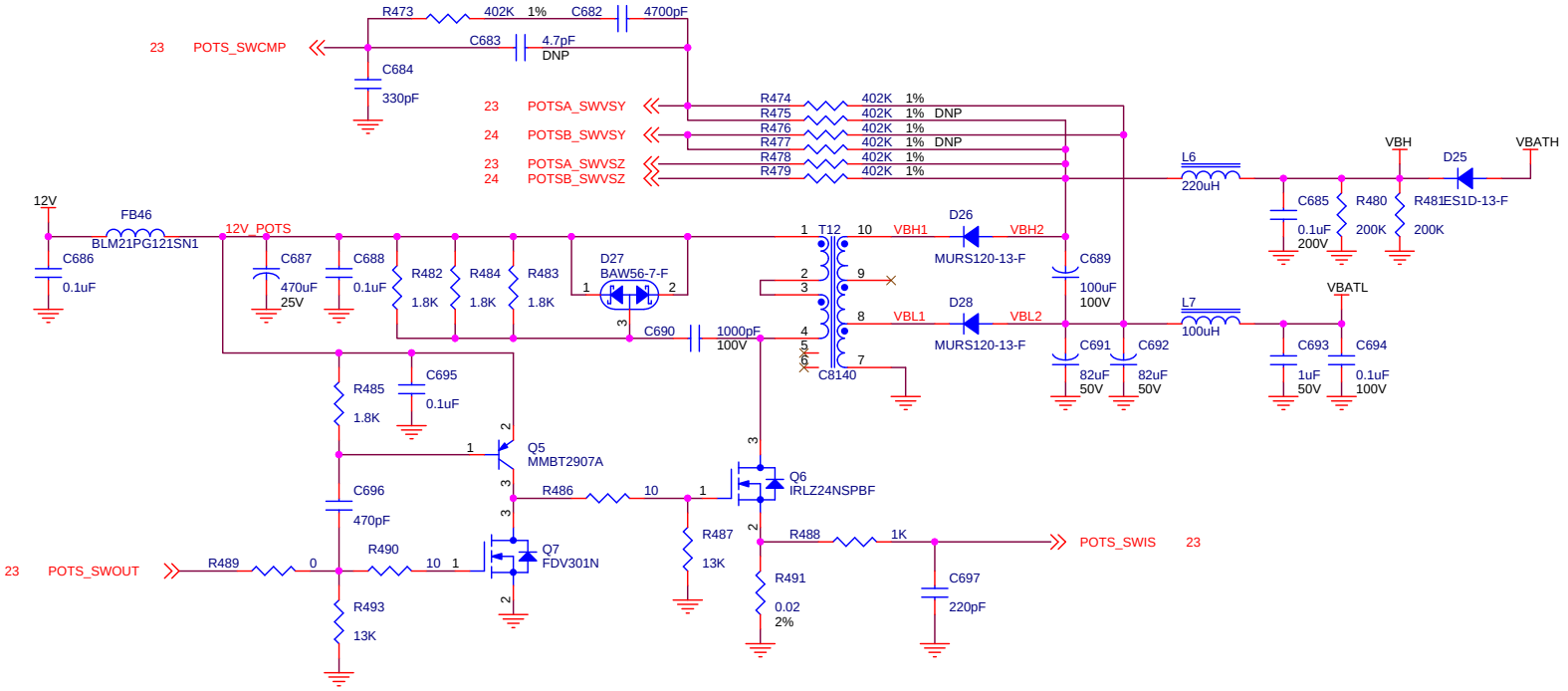
POTS VBAT POWER SUPPLY

T1040 ONLY!



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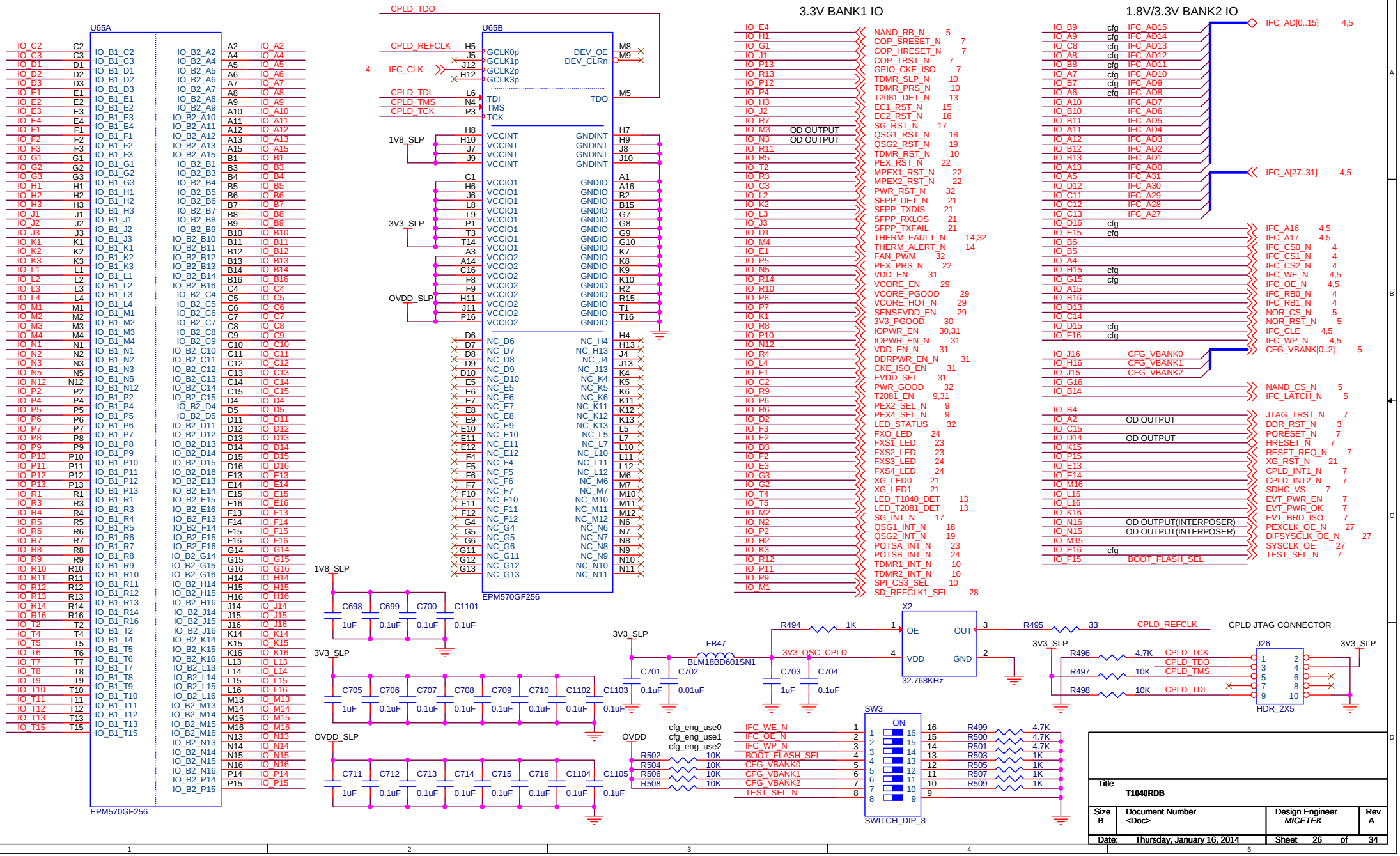
CPLD


U65A
EPM570GF256
U65B
EPM570GF256
CPLD_TDO
CPLD_REFCLK
IFC_CLK
CPLD_TDI
CPLD_TMS
CPLD_TCK
1V8_SLP
3V3_SLP
OVDD_SLP
3.3V BANK1 IO
1.8V/3.3V BANK2 IO
IFC_AD[0..15]
IFC_A[27..31]
CFG_VBANK[0..2]
X2
32.768KHz
FB47
BLM18BD601SN1
SW3
SWITCH_DIP_8
CPLD JTAG CONNECTOR
J26
HDR_2X5
Title
T1040RDB
Size B
Document Number <Doc>
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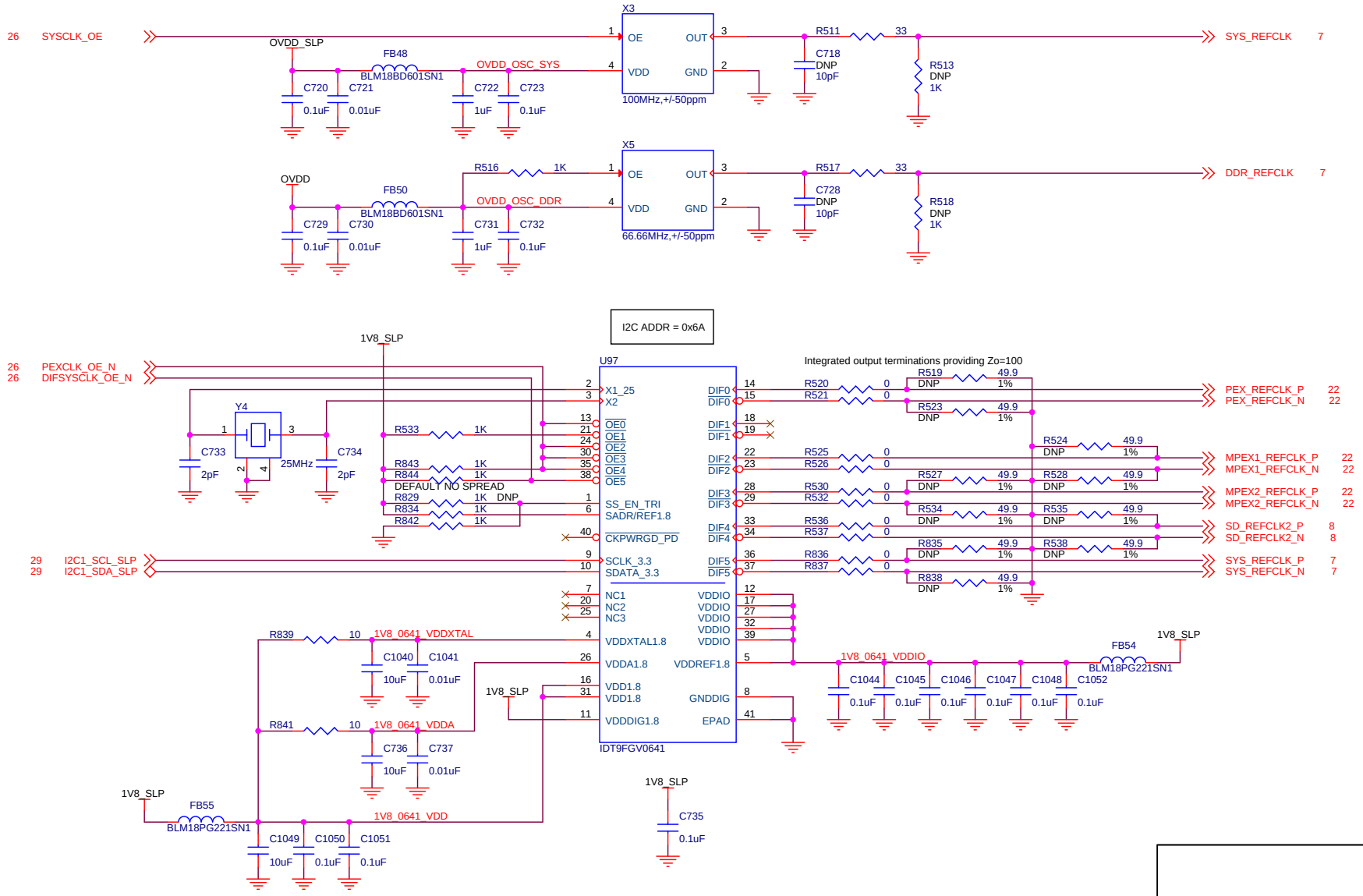
SYSTEM CLOCK GENERATORs



Title: T1040RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
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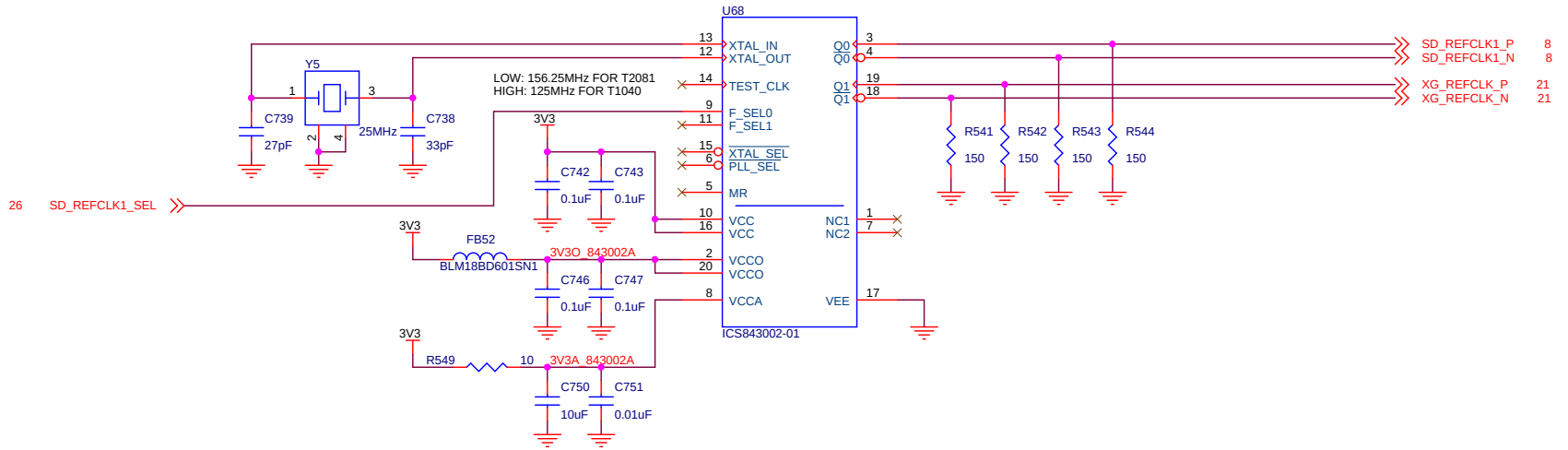
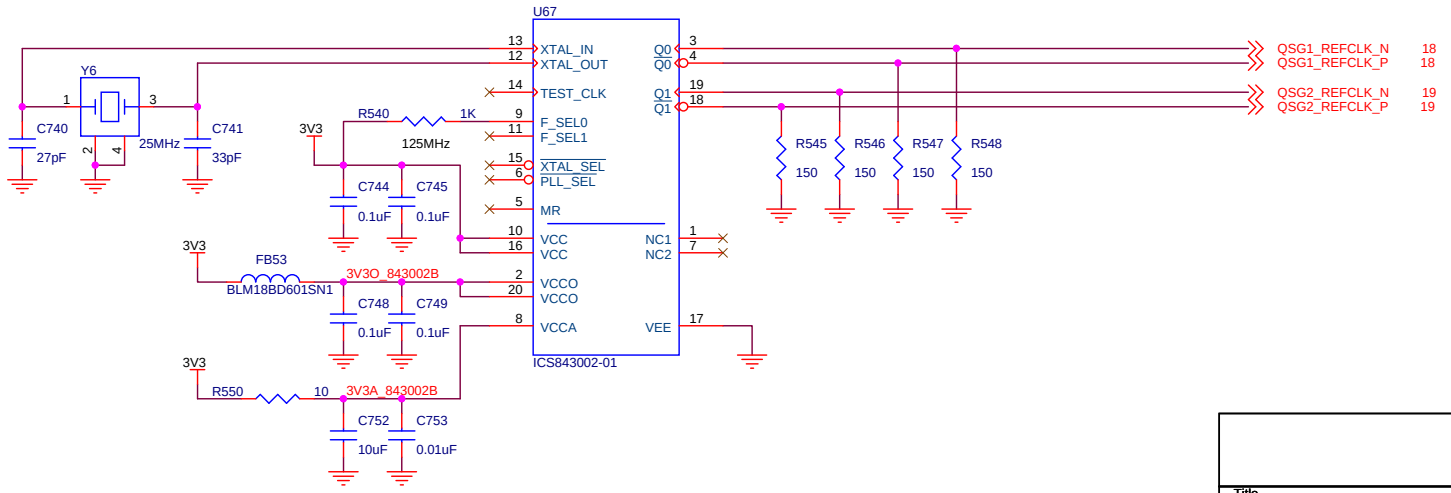
SYSTEM CLOCK GENERATORs (cont.)



T1040 ONLY!



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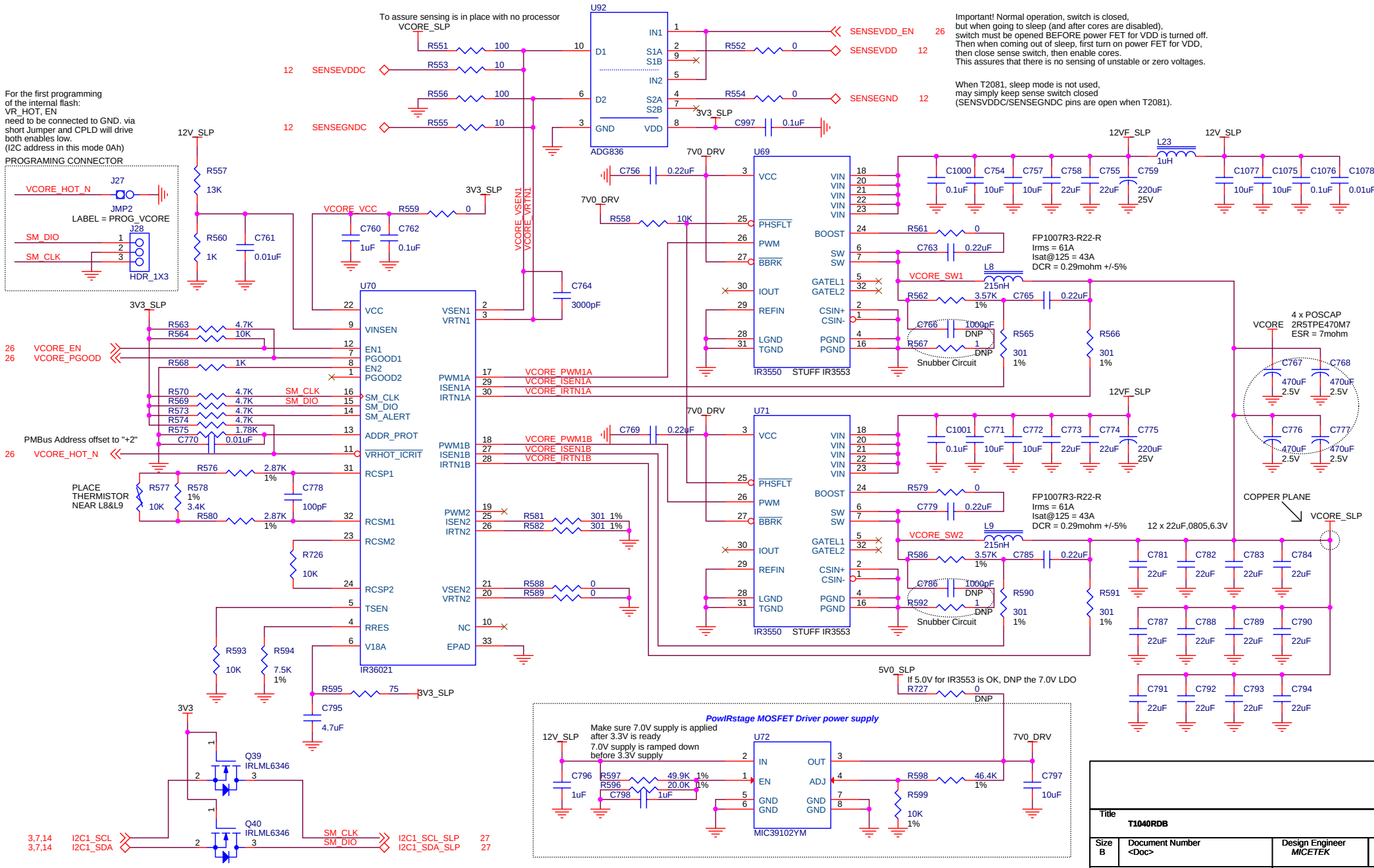
T1040 CORE POWER CONVERTOR



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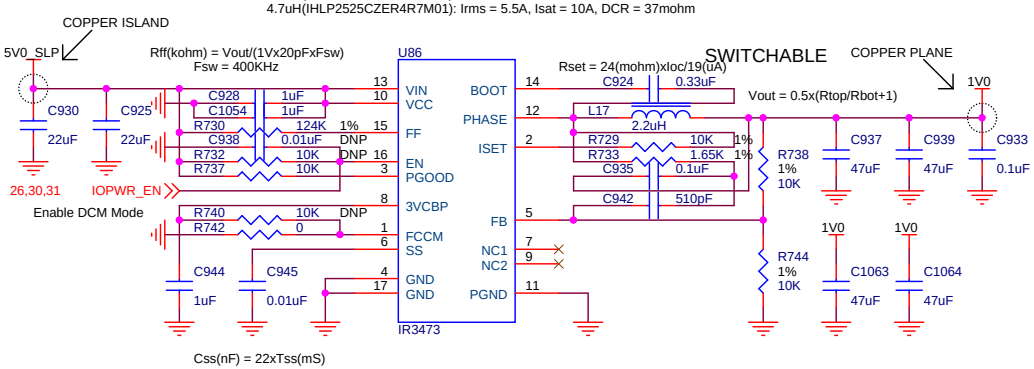
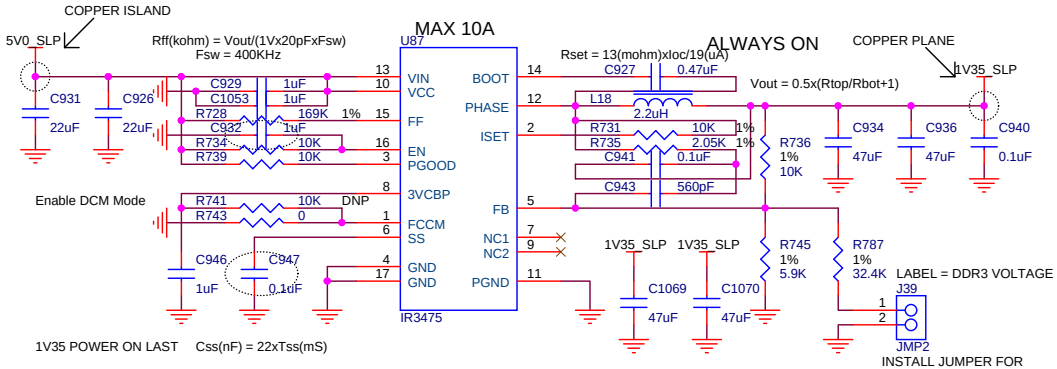
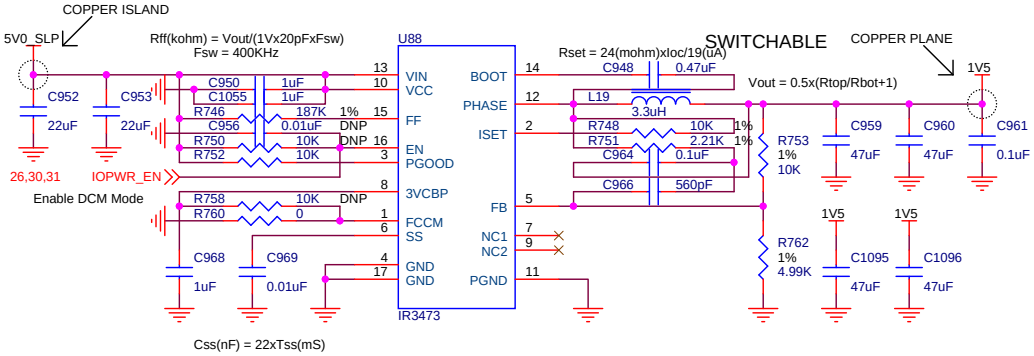
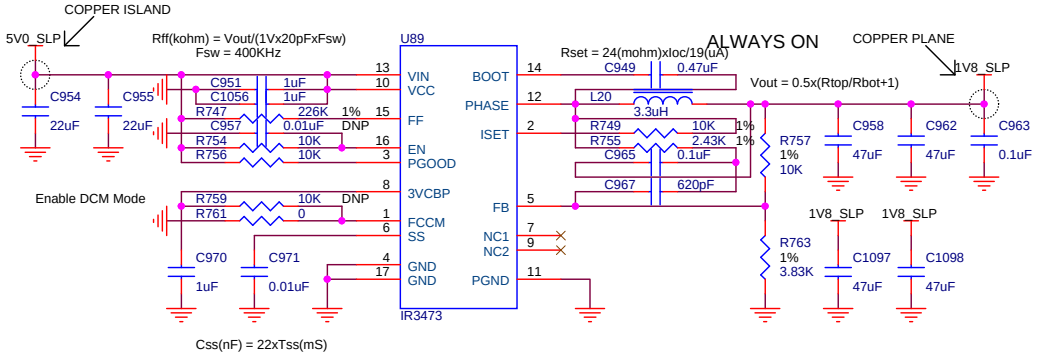
SYSTEM POWER CONVERTORs

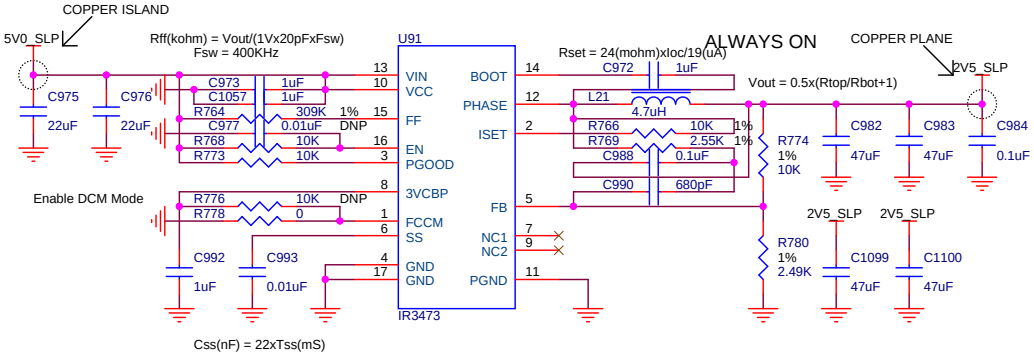
2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

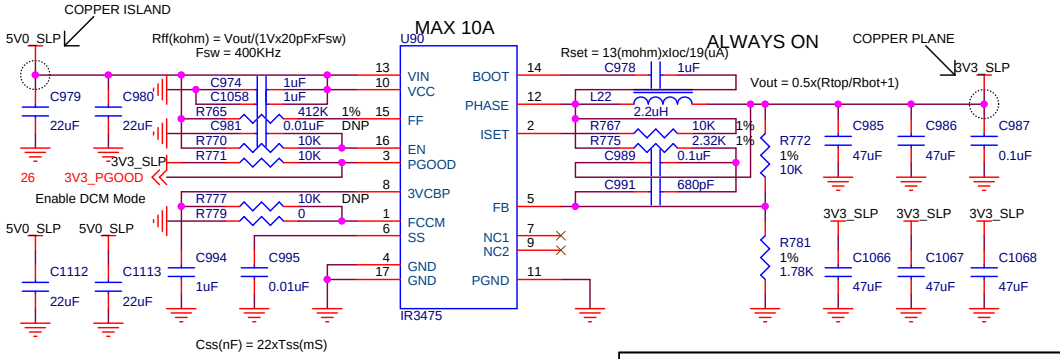












Caution: separate analog and power ground and make connection at GND plane

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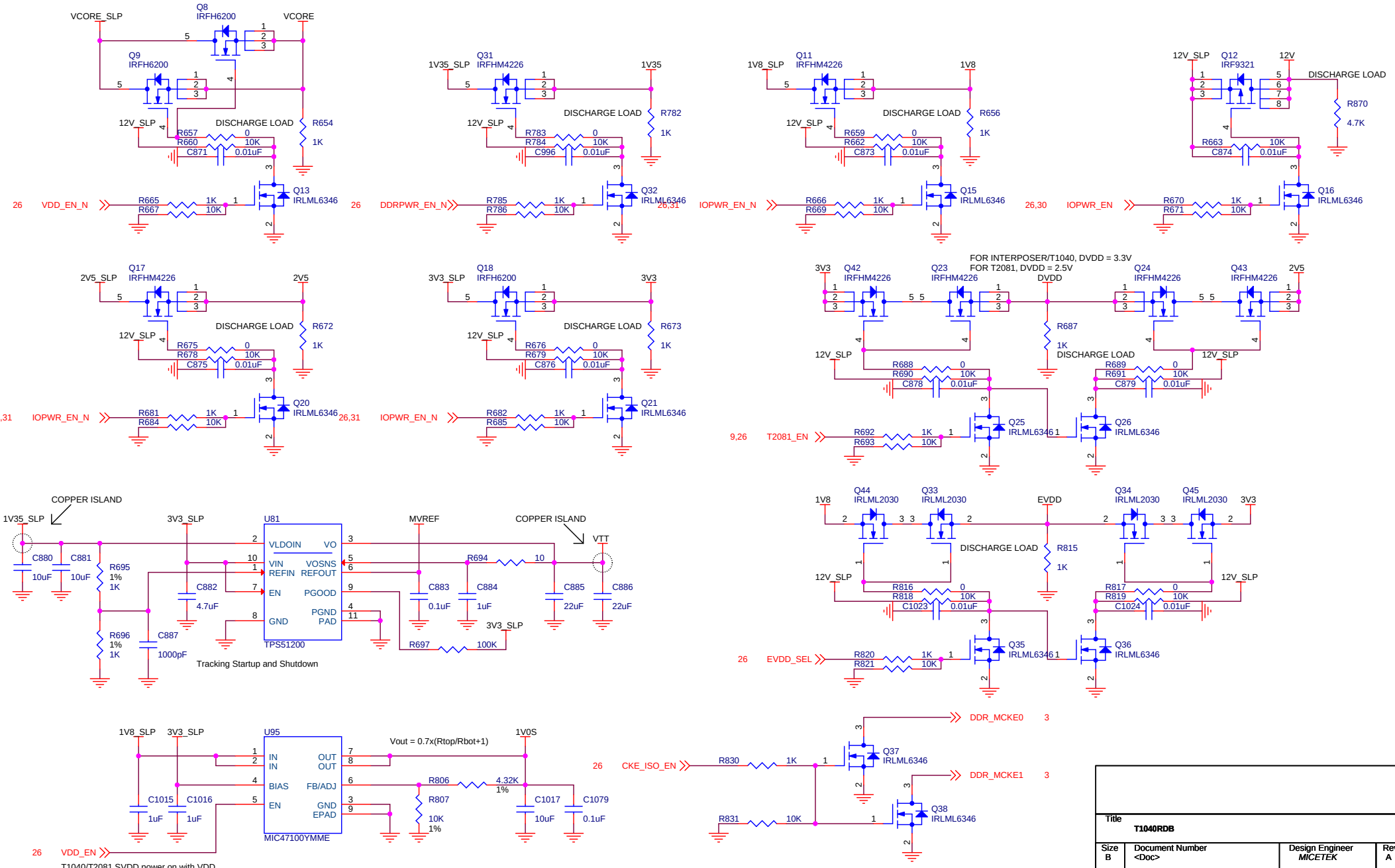
SYSTEM POWER SWITCHs



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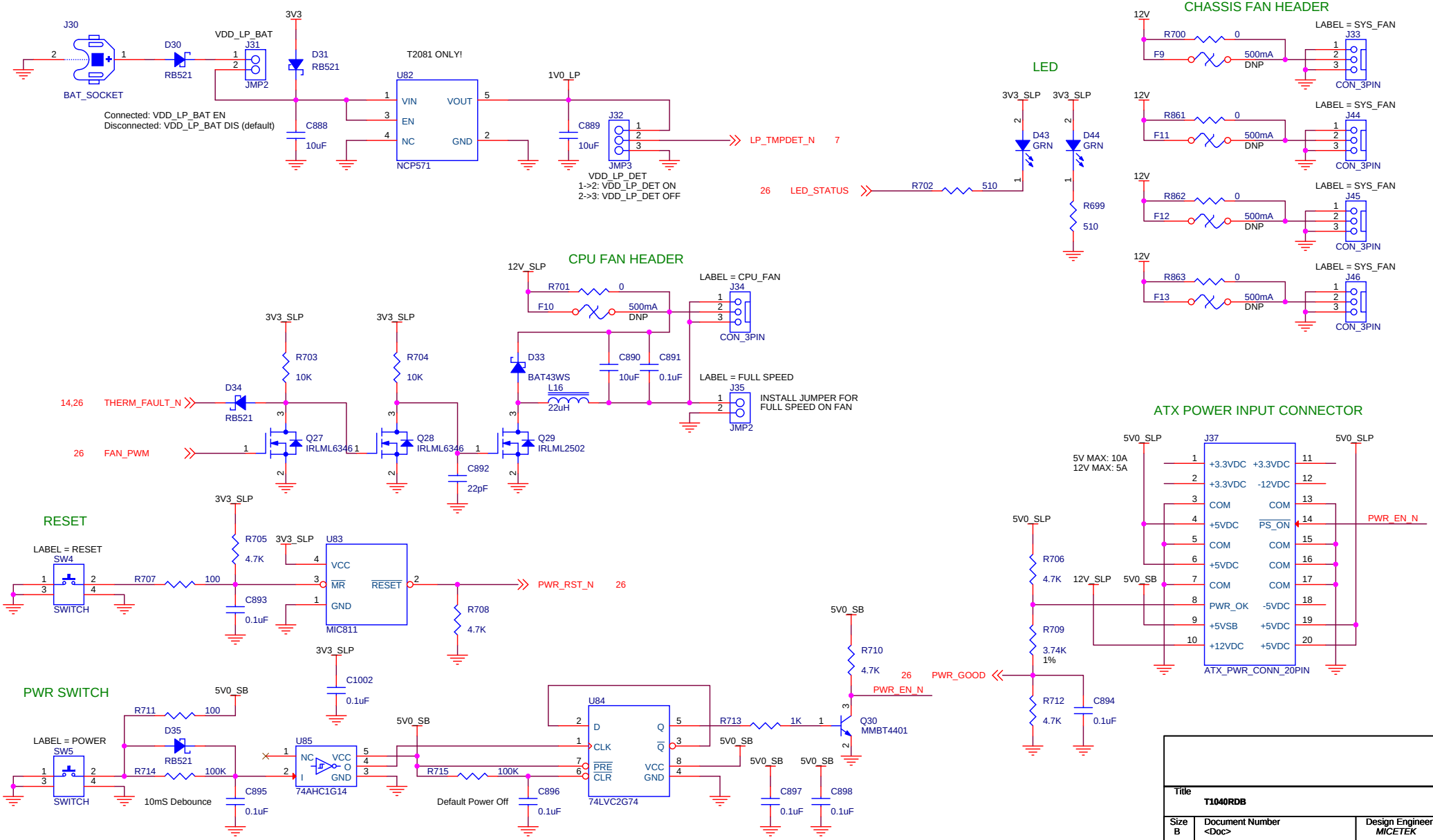
SYSTEM POWER INPUT



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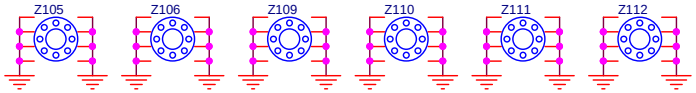
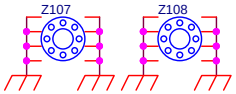
MECHANICALs

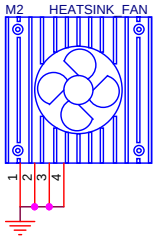
Fiducial Marks

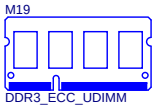
Mouting Holes





Heatsink Fan





DDR3_ECC_UDIMM
Micron MPN(4GB,1600): MT18KSF51272AZ-1G6

Layer Detail

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CHANGE LIST

2013/6/12
1. Add DDR3 CKE pull down circuit for deep sleep
2. Change SYSCLK to 66.66MHz and DDRCLK to 133.33MHz
3. Change ICS557-05 S0~S2 configuration to support spread, but default no spread
4. Change power switch mosfet to IR
5. Add dip switch for board configuration form CPLD, but bit definition need to confirm

2013/6/13
1. Add 100MHz diff SYS_CLK to support single source clock input mode
2. Change SD card WP pin ESD protect circuit

2013/6/14
1. Correct JTAG_TRST_N single pin error
2. Change 1 MOSFET of VDD switch to 2 for decrease Rds-on

2013/6/17
1. Use Mux/Demux for SerDes to switch T1040/T2081
2. Change DVDD voltage select by MOSFET
3. Change 2N7002 MOSFET to IRLML6346
4. Change CVDD and EVDD connect to OVDD, add voltage translator to SPI and SDHC
5. Delete INTERPOER_N signal
6. Change FXO 2PIN connector to RJ11
7. Change DIN power connector to 20PIN ATX power connector
8. Correct 2V5 power DCDC chip from IR3898 to IR3897
9. Change low current MOSFET from IRFH6200 to IRLHM620
10. Change VCORE DCDC to IR36021
11. Add front panel LEDs
12. Add 3V3_PGOOD to CPLD for power-on reset

2013/6/19
1. Change EMI2 pull-up resistor to 270ohm for MDC and 510ohm for MDIO(pull-up to 1.8V)
2. Add MOSFET for USB PWRFAULT signal active high
3. Change ICS557-05 to IDT5V41236 for PCIE GEN2 and GEN3 support
4. Correct NCP1117 resistor value

2013/6/21
1. Update PRO config signals connection
2. Change CPLD from EPM240G to EPM570G

2013/6/22
1. Delete unused IFC_AD0~4 to 74LVC16373
2. Update IR36021 VCORE circuit

2013/6/23
1. Add T1040/T2081 detect LED
2. Add labels for LEDs and connectors
3. Add voltage translator for UART signals

2013/7/5
1. Change SD_REFCLK1 to 156.25MHz and SD_REFCLK2 to 100MHz
2. Change IRLHM620 to IRFHM4226
3. GVDD and USB power do not need to turn off
(GVDD: 1V35_SLP for GVDD, delete MCKE pull-down circuit, delete MVREF_SLP MOSFET,
change AVDD_D1 to 1V8_SLP)(USB: change USB_SVDD,USB_HVDD,USB_OVDD power to SLP power)
4. Change IR3897 and IR3898 to IR3473 or IR3475
5. Add 5V0_SLP to 7V0_DRV option for LDO cost
6. Change IR36021 programing connector pin order
7. Delete RCSP/RCSM temp sense circuit for loop2 of IR36021
8. Add more 10uF caps for VDDC and VDD
9. Update VSC8514 circuit refer to reference design

2013/7/7
1. Correct SD_TX/RX1 Mux/DeMux control pin connection
2. Change Mux/DeMux chip from PI3PCIE3215 to PI3PCIE3212,delete bead of power supply,change caps to 0.01uF
3. Add 2pin jumper for DDR3 voltage change to 1.5V surport
4. Add 2pin 2mm wafer CPU_FAN connector
5. Add front panel connector and LED connector

2013/7/12
1. Add analog switch for sense VDDC or VDD select

2013/7/13
1. Correct IR3473 connection error
2. Change IR36021 programing connector pin order

2013/7/19
1. Add 20K pull-up to IFC_A[16-19],AVD,OE,WE,WP
2. Add IFC_LATCH_N to IFC voltage level translators
3. Change NAND RB pull-up to 1K
4. Change SD card ESD chip to Rclamp0524J
5. Change NOR MPN to S29GL01GP11TFIV10
6. Add 1.0V LDO for S1VDD, use NFM55PC155F1H4B instead of BLM18 bead for SVDD and XVDD
7. Change SD card insert and protect signal pull-up to 1.8V and connect to T2080 derectly

2013/7/24
1. Connect EVT2, EVT3, EVT9, IRQ9 to CPLD for sleep mode control
2. Change I2C MUX address to 0x77
3. Add test point for CLK_OUT and RTC, change RTC pull-down to 10K
4. Add test point for 1588 signals
5. Change USB protect chip from SRV05-4 to VBUS054B-HSF
6. Change LED drive resistor from 330ohm to 510ohm
7. Correct VSC8514 QSGMII TX/RX pin out error
8. Add MCKE pull-down circuit
9. Add EVDD select circuit, SDHC support 1.8V or 3.3V, change SDHC_CLK serial resistor to 0 ohm
10. Add test points for SD_PLL_TPA and SD_PLL_TPD
11. Add optional filtering for USB_BIAS
12. Connect RGMII PHY tap pins together, change crystal caps from 20pF to 27pF,
remove bead, add 0 ohm to ENSWREG, change RST to pull-up

2013/7/30
1. Change the VDD/VDDC sensing strategy
2. Change sleep mode enter or exit power control signals to 3 tiers
(general IO power, core power, DDR power)
and CKE isolate control signal, correct IRQ9 and EVT9 signal name
3. Change GND CKE chip from 74LVC1G125 to MOSFET

2013/8/2
1. Change EVDD switch signal to IRQ3 though CPLD(1.8V<->3.3V), delete SGMII PHY PME interrupt
2. Change SVDD and XVDD power enable signal belong to VCORE and GVDD
3. Change SVDD LDO from MIC49150 to MIC47100

2013/8/5
1. Change IDT5V41236 to IDT9FGV0641 to support single source clock
2. Delete differential output OSC of system clock

2013/8/8
1. Add 1uF input cap to IR3473/IR3475
2. Change all IR3473 OCP resistor to 10K

2013/8/15
1. Change SYS_REFCLK to 100MHz
2. Update IR3473/IR3475 circuit
3. Change SVDD and XVDD filter cap from NFM55PC155 to NFM21PC225

2013/8/20
1. Delete backpanel LEDs, LED header and front panel header

2013/8/23
1. Add SE SYSCLK and DIFF SYSCLK select control from CPLD, OD output for IDT9FGV0641(1.8V)
2. Isolate I2C1 for don't sleep chips

2013/9/4
1. Change PMC connector to TDM riser card connector
2. Change IRQs to CPLD then CPLD to T1040/T2081

2013/9/11
1. Change DDR3 SODIMM to UDIMM

2013/9/12
1. Add notes at page 1
2. Change DDR REFCLK from 133.33MHz to 66.66MHz

2013/9/27
1. Update system block diagram
2. Change DVDD and EVDD power select from 1 MOSFET to 2 MOSFET

2013/10/8
1. Change VCORE caps near T1040 from 10uF to 22uF

2013/10/10
1. Add 51ohm resistors for SPI signals
2. Change VCORE caps near T1040 to follow QDS board

2013/10/19
1. Add GVDD power-on delay
2. Correct 12V enable signal name
3. Add 2x22uF to 3.3V DCDC power input

2013/11/19
1. Change QSGMII PHY MPN

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